EDSSC 17TH 2026

The 17th IEEE International Conference on Electron Devices and Solid-State Circuits

Conference Program

June 9-12, 2026 Guangzhou, China

◇ Sponsors ◇

IEEE Guangzhou Section

South China University of Technology

IEEE Hong Kong ED/SSC Joint Chapter

Important Notes

1. This conference handbook provides essential information for delegates and is for reference during the conference. For additional details, schedule changes, or impromptu events, please refer to notifications issued by the Conference Secretariat.

2. The Guest Pass/Participant Pass collected upon registration serves as your credential. Please wear it visibly and keep it secure throughout the conference.

3. Please adhere to conference regulations. Arrive at the session venue 10-15 minutes early and be seated in designated areas.

4. To maintain a conducive environment, please set mobile phones to silent mode, refrain from loud conversations inside session halls, and do not smoke in conference areas or other designated non-smoking zones.

5. Presentation slides should ideally be in 16:9 format. Please submit your PPT files to the Conference Secretariat for centralized uploading onto the venue computers.

6. Presenters should prepare in advance and strictly adhere to the allotted time in the agenda. Staff will provide a 5-minute warning before your time expires.

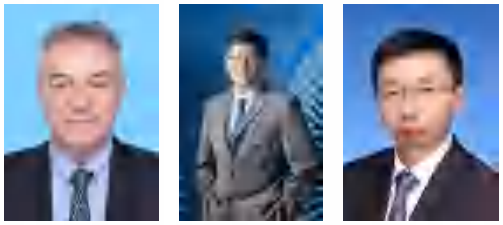
7. Please take full responsibility for securing your personal valuables during the conference.

8. Registration fees are non-refundable for early departure due to special circumstances. Your understanding is appreciated.

9. For assistance, please contact conference staff wearing official credentials clearly marked “STAFF”.

Welcome Message From the General Chairs:

Dear colleagues, researchers, and friends,



As General Chairs of the 17th IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC 2026), it is our great honor and genuine pleasure to welcome you to Guangzhou — a dynamic global hub of innovation and technology.

From June 9 to 12, 2026, we gather together to share discoveries, spark collaborations, and shape the future of electron devices and circuits.We extend our deepest gratitude to our sponsors and hosts — the IEEE Guangzhou Section, the South China University of Technology, and the IEEE Hong Kong ED/SSC Joint Chapter. Their steadfast support has made this conference possible and truly exceptional.

The technical program you will experience reflects the remarkable breadth of our community. This year, we feature cutting-edge contributions across a wide spectrum, including nanoelectronics, memory technologies, RF and microwave devices, power devices, analog and digital circuits, biomedical circuits, power management, EDA, AI, and emerging device architectures. Every accepted manuscript has undergone a rigorous peer-review process, ensuring the highest standards of originality and technical impact.

We sincerely thank our Technical Program Committee Chairs — Changjian Zhou, Yanjie Wang, Yang Chai, Wai Tung Ng, Kong Pang Pun, Xiwen Liu, Yun Wang, and Yuan Liu — for their dedication and scholarly judgment. We also appreciate the hard work of our Publication Chairs, Local Arrangement Chairs, Publicity Chairs, International Advisory Committee, and all volunteers who have worked tirelessly behind the scenes.

But a conference is more than papers and sessions — it is a living community. So we warmly invite you to do more than just attend. Ask bold questions. Introduce yourself to someone whose work inspires you. Share your ideas over coffee. Seek out collaborators across disciplines and borders. Whether you are a seasoned expert or a first-time presenter, this conference belongs to you.

Welcome to Guangzhou — a city where tradition meets tomorrow, where world-class laboratories sit beside the beautiful Pearl River, and where you will find both excellent science and warm hospitality.

Welcome to EDSSC 2026 — together, let us ignite new ideas and advance the frontiers of electron devices and solid-state circuits.

Sincerely,
EDSSC 2026 General Chairs

Venue and Schedule Overview

Time	Activity	Venue
June 9 (Tuesday)		
13:00-18:00	On-site Registration	Lobby, 3F
14:00-17:00	Academic Conference Tutorial	Meeting Room1, 3F
June 10 (Wednesday)		
09:00-12:00	Opening and keynote	Main Hall, 3F（三楼宴会厅1+2）
12:00-13:30	Lunch Buffet	三楼宴会厅3
13:30-15:10	Session 1: Digital and Memory Circuits	Meeting Room 1, 3F
	Session 2: ADCs and Power Management Circuits-1	Meeting Room 2, 3F
	Session 3: Nanoelectronics-1	Meeting Room 3, 3F
	Session 4: Memory Devices and Tech-1	Multifunction Room, 3F
15:10–15:30	Coffee Break	
15:30–17:10	Session 5: Biological and Sensing Circuits and Devices	Meeting Room 1, 3F
	Session 6: ADCs and Power Management Circuits-2	Meeting Room 2, 3F
	Session 7: Power Devices-1	Meeting Room 3, 3F
	Session 8: Memory Devices and Tech-2	Multifunction Room, 3F
18:30–21:00	Welcome Reception	三楼宴会厅1

Venue and Schedule Overview

Time	Activity	Venue
June 11 (Thursday)		
09:00-11:15	FET 100	Multifunction Room, 3F
11:15-12:15	Poster Session 1	Multifunction Room, 3F
12:15-13:30	Lunch Buffet	三楼白鹭轩西餐厅
13:30-14:55	Session 9: Analog and Communication Circuits	Meeting Room 1, 3F
	Session 10 : RF and Microwave Circuits and Devices-1	Meeting Room 2, 3F
	Session 11: Integrated Silicon Photonics and High-Performance Photodetectors	Meeting Room 3, 3F
	Session 12: Wide-Bandgap Semiconductors: Contacts, Devices, and Reliability	Multifunction Room, 3F
14:55-15:10	Coffee Break	
15:10-16:30	Session 13: Emerging Sensors and Neuromorphic Devices	Meeting Room 1, 3F
	Session 14 : RF and Microwave Circuits and Devices-2	Meeting Room 2, 3F
	Session 15: Nanoelectronics	Meeting Room 3, 3F
	Session 16: Process Design and Device Modeling	Multifunction Room , 3F
16:30-17:30	Poster Session 2 / Lab Tour to SCUT	Multifunction Room, 3F
18:30 – 21:00	Dinner Buffet	三楼白鹭轩西餐厅

Venue and Schedule Overview

Time	Activity	Venue
June 12 (Friday)		
09:00-10:25	Session 17: Device Reliability	Meeting Room 1, 3F
	Session 18: EDA And AI-1	Multifunction Room, 3F
10:25-10:40	Coffee Break	
10:40-12:05	Session 19: Display and Imager	Meeting Room 1, 3F
	Session 20: EDA And AI-2	Multifunction Room, 3F
12:05–13:00	Lunch Buffet	三楼白鹭轩西餐厅

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Conference Introduction

Conference Introduction

Welcome to the 17th IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC 2026)

On behalf of the Organizing Committee, it is our great pleasure to welcome you to the 17th IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC 2026), held in the vibrant and dynamic city of Guangzhou, China, from June 9-12, 2026.

As the 17th edition in this flagship series initiated by the IEEE ED/SSC Beijing Section Hong Kong Chapter, EDSSC has established itself as a premier international forum for researchers, academics, and industry professionals. Continuing this proud tradition, EDSSC 2026 provides a multidisciplinary platform dedicated to the exchange of groundbreaking ideas, the sharing of cutting-edge research results, and the discussion of industry trends within the expansive fields of electron devices, solid-state circuits, and systems.

A Dynamic Program in a Leading Hub

Hosted by the prestigious South China University of Technology, this year's conference features a rich technical program. Attendees can look forward to compelling invited talks from distinguished scientists and pioneers, alongside presentations of contributed papers covering the full spectrum of the field. The technical scope is comprehensive, inviting the latest contributions on topics ranging from fundamental nanoelectronics, memory, and RF devices to advanced analog, power management, and communication circuits, as well as emerging intersections like EDA and Artificial Intelligence (AI).

Publication and Indexing

All accepted and presented papers will be submitted for inclusion in the IEEE Xplore digital library, one of the world's leading collections of technical literature in electrical engineering and computer science. Furthermore, these papers will be indexed by EI Compendex, ensuring high visibility and recognition within the global academic community.

A Commitment to Excellence

We extend our sincere gratitude to our sponsors—the IEEE Guangzhou Section, the South China University of Technology, and the IEEE Hong Kong ED/SSC Joint Chapter—for their unwavering support. We also acknowledge the dedication of our distinguished General Chairs, Technical Program Committee, and all organizing committees whose efforts have shaped this event.

We are confident that EDSSC 2026 will be a rewarding and memorable experience, fostering collaboration and inspiring future innovations. Welcome to Guangzhou, and enjoy the conference!

Organized by:

IEEE Guangzhou Section

South China University of Technology

IEEE Hong Kong ED/SSC Joint Chapter

For more information, please visit the official conference website: http://www.ieee-edssc.org

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Organizing Committee

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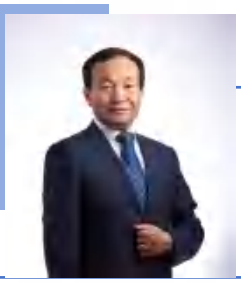
Keynote Speakers

Keynote Speakers



Prof. Dapeng Yu

International Quantum Academy, China

Biography

Prof. Dapeng Yu, Academician of the Chinese Academy of Sciences and Fellow of the American Physical Society (APS), is currently a professor at the School of Physics, Peking University, and the president of the Shenzhen International Quantum Academy. He also serves as the chairman of the Quantum Information Society of the Chinese Institute of Electronics.

He has long been engaged in research on quantum computing, quantum state control of condensed matter, and the development of key core scientific instruments in the field of quantum information. In recent years, Prof. Yu's main research has focused on the precise quantum control of quantum phases of matter, achieving a series of significant research results with substantial international impact and making major breakthroughs in the independent development of several scientific instruments.

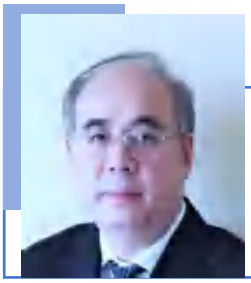
Speech Title

Everything is Quantizable:Quantum Computing is Everyone's Responsibility

Abstract

Quantum mechanics describes the most fundamental layer of physical reality—the set of rules governing how everything in the universe behaves. In that sense, at its core, "everything is quantum." Quantum computing is the ambitious endeavor to harness these rules, representing one of the most demanding engineering challenges of our time. It pushes the boundaries of our ability to control the microscopic world and could ultimately unleash the disruptive computational power needed to drive the next industrial revolution. As the saying goes, "Every craftsperson needs the right tools." This report begins with a brief introduction to the Shenzhen International Quantum Institute. It then turns to the current state of the quantum information industry, both in China and globally, and underscores why scientific instrumentation, self-reliance, and independent R&D are critical to success in this field.

Keynote Speakers



Prof. Wei Hong

Southeast University, China

Biography

Wei Hong received the B.S. degree from the University of Information Engineering, Zhengzhou, China, in 1982, and the M.S. and PhD degrees from Southeast University, Nanjing, China, in 1985 and 1988, respectively, all in radio engineering.

He is currently a professor of the School of Information Science and Engineering, Southeast University. In 1993, 1995, 1996, 1997 and 1998, he was a short-term visiting scholar with the University of California at Berkeley and at Santa Cruz, respectively. He has been engaged in numerical methods for electromagnetic problems, millimeter wave and terahertz theory and technology, antennas, RF technology for wireless communications etc. He has authored and co-authored over 400 technical publications and 5 books. He twice awarded the National Natural Prizes of China, once awarded the National Science and Technology Progress Award, four times awarded the first-class Science and Technology Progress Prizes issued by the Ministry of Education of China and Jiangsu Province Government, and 2021 IEEE MTT-S Microwave Prize etc.

Dr. Hong is a Fellow of IEEE, Fellow of CIE, the vice presidents of the CIE Microwave Society and Antenna Society, and was an elected IEEE MTT-S AdCom Member during 2014-2016, served as the Associate Editor of the IEEE Trans. on MTT from 2007 to 2010.

Speech Title

Research Progress in Terahertz Devices, Chips, and Systems

Abstract

In this talk, the recent research progress in terahertz (THz) devices, chips and systems in the State Key Laboratory of Millimeter Waves (SKLMMW) of Southeast University and cooperative enterprises are reviewed.

Keynote Speakers

Prof. Tianchun Ye

University of Chinese Academy of Sciences, China

Biography

Tianchun Ye, born in 1965, he is an IEEE Fellow and a graduate of the Department of Electronic Engineering at Fudan University. He previously served as the Director of the Institute of Microelectronics, Chinese Academy of Sciences, and led a National Science and Technology Major Project. He has received three National Technology Invention Awards and four First-Class Invention Awards at the ministerial and provincial levels. Leading his team in over a decade of persistent research, he proposed a series of innovative technical methodologies and achieved multiple major inventions at the forefront of international standards. These technologies have been adopted by leading enterprises both in China and abroad for the mass production of cutting-edge products, making pioneering contributions to the self-reliance and development of China's advanced integrated circuit processes.

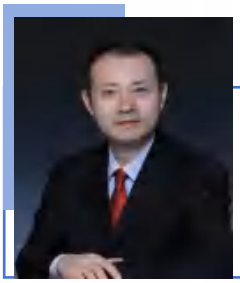
Speech Title

Technology Innovation in Integrated Circuit Transistor Process

Abstract

Integrated circuit process evolution is the fundamental basis for the development of modern information and artificial intelligence technologies. Over the past few decades, China has been making continuous efforts in this field. Starting from the 90nm node, integrated circuit CMOS transistors have demanded the development of new processes, materials, and structures to overcome key bottlenecks in PPA scaling by generations. The Institute of Microelectronics of the Chinese Academy of Sciences (IMECAS) has long been engaged in the research and development of innovative transistor technologies. They have made a great breakthrough on technical challenges such as precise gate control, transistor performance modulation, and structural scaling in both 22nm high-k/metal gate-last, 14nm FinFET, and up-to-date GAA transistor processes, established a technical system with comprehensive independent intellectual property rights, and successfully applied it to domestic and international cutting-edge integrated circuit products.

FET 100-Speakers



Prof. Tian-Ling Ren

Tsinghua University, China

Biography

Prof. Tian-Ling Ren is a distinguished professor at Tsinghua University. He serves as Vice Dean of the School of Information Science and Technology, and Director of the Tsinghua University-BEIGC Joint Research Center. He is IEEE Fellow, and Chinese Society of Micro-Nano Technology Fellow.

His research focuses on intelligent micro-nano electronic devices, 2D nanoelectronic devices, flexible wearable systems, and intelligent sensing chips. He has led many national key research projects and achieved world-renowned innovations, including the world's shortest gate-length transistor, the first graphene intelligent artificial throat, high-performance flexible AI chips, and intelligent healthcare systems.

He has published over 900 papers in top journals and conferences, such as Nature and IEDM, with more than 30,000 Google Scholar citations. He holds more than 200 patents and has been selected as an Elsevier Highly Cited Researcher for consecutive years.

Speech Title

Novel Device and Chip Technologies Driving Moore's Law

Abstract

As Moore's Law faces severe physical bottlenecks—including thermal and quantum mechanical limits—sustaining the exponential growth of integrated circuits requires innovations beyond simple dimensional scaling. This talk presents recent advances in novel device and chip technologies that both extend and go beyond Moore's Law. In the extending direction, we demonstrate a sub-1nm gate-length transistor with a physical gate length of only 0.34 nm using a graphene edge gate and a MoS_2 channel, pushing device scaling to the atomic limit. We also introduce flexible inmemory computing chips that achieve high clock frequency and energy efficiency, enabling edge computing on conformable substrates. In the beyond-Moore direction, we highlight smart graphene-based artificial throats that restore voice communication for laryngectomees, and a motion-artifact-free 12-lead dynamic ECG system with onchip AI processing for unobtrusive, continuous cardiac monitoring. These developments illustrate that novel devices enabled by low-dimensional materials and flexible electronics can effectively promote Moore's Law with wide intelligent healthcare and human-machine interface applications.

FET 100-Speakers

Prof. Pui-In Mak

University of Macau, China

Biography

Pui-In Mak is Chair Professor at the University of Macau, Macau, China, Director of the State-Key Laboratory of Analog and Mixed-Signal VLSI, and Director of the Guangdong-Macao Joint Laboratory for Modular Chip Design and Testing. His research interests are on analog and radio-frequency circuits and systems for wireless and multidisciplinary innovations. He received the Xplorer Prize in 2022, and is recognized as one of the Top Contributing Authors of ISSCC at its 70th anniversary in 2023, and the Medal of Merit-Education from the Macau government in 2024. He is currently AdCom Member of the IEEE Solid-State Circuits Society and Editor-in-Chief of the IEEE Solid-State Circuits Letters, and was an Associate Editor of the IEEE Journal of Solid-State Circuits. He is a Changjiang Scholar, Overseas Expert of the Chinese Academy of Sciences, Fellow of the IEEE, IET and UK Royal Society of Chemistry. He is a foreign academician of the Academy of Sciences of Lisbon (ACL), Portugal.

Speech Title

The Frontiers of Microelectronic Engineering over the Next Decade

Abstract

This talk explores the transformative landscape of microelectronic engineering over the next decade. As we navigate advancements in integrated circuits (IC) with artificial intelligence (AI), we will highlight emerging trends that promise to redefine the experience of humans interact with their surroundings that will be collectively proactive, and highly personalized. Key topics will include the embodiment of power-efficient edge AI chips in wearables/robots, ultra-low-power radio chips for battery-free wireless connectivity, and easy-to-use advanced instruments, shifting towards a highly-efficient healthcare home system. By examining the current challenges and opportunities of IC+AI, this presentation aims to envision a future where microelectronics plays a pivotal role in re-shaping our quality of life. Join us as we delve into the frontiers that will surf on the next big wave of engineering breakthroughs.

FET 100-Speakers

Prof. Han Wang

University of Hong Kong, China

Biography

Han Wang is a Professor in the Department of Electrical and Computer Engineering at the University of Hong Kong (HKU). He also serves as the Director of HKU Center for Advanced Semiconductors and Integrated Circuits and Co-Director of the Institute of Mind at HKU. Prior to joining HKU, he was tenured Associate Professor at the University of Southern California. In 2021-2023, he served as the Head of New Material and Device Research department at Taiwan Semiconductor Manufacturing Company (TSMC), concurrent to his faculty appointment. He has also served as the Chair of the IEEE EDS Neuromorphics Technical Committee and Chair of the IEEE ED/SSC Hong Kong Joint Chapter.His work has been recognized with numerous prestigious awards including the IEEE IEDM Roger A. Haken Best Paper Award, US NSF CAREER Award, IEEE Nanotechnology Council Early Career Award, the US Army Research Office Young Investigator Award. He is the IEEE Nanotechnology Council Distinguished Lecturer and the Clarivate Highly Cited Researcher for eight consecutive years 2018-2025. Prof. Wang is a Fellow of IEEE.

Speech Title

CMOS Technology in the Nanoscale Era

Abstract

This talk provides an overview of the evolution of CMOS technology, tracing its remarkable journey from the early logic gates of the 1970s to today's advanced nodes and beyond. The first part reviews key historical milestones—including the scaling principles of Dennard and Moore, the transition from planar to FinFET devices, and the introduction of strain engineering, and highk/metal gates—that have sustained performance and density gains over five decades.

The second part focuses on future development directions for advanced-node CMOS. It examines emerging device architectures such as nanosheet GAAFETs, forksheet FETs, and CFETs, along with novel channel materials (2D semiconductors, Ge, etc.). On the integration front, the talk discusses monolithic and hybrid 3D integration and backside power delivery networks. Challenges related to power density, variability, interconnect delay, and lithography extensibility will be highlighted. The talk concludes with a forwardlooking perspective on how emerging technologies will shape the next decade of CMOS innovation.

Conference Agenda

Conference Agenda

Academic Conference Tutorial

Time	Activity
June 9 (Tuesday) 14:00-17:00 Venue: Meeting Room1, 3F	
Chair: Shaolin Zhou	
14:00-15:00	Speaker: Kong-Pang PUN, The Chinese University of Hong Kong Title: *Design of Bandpass Delta-Sigma Modulators Based on N-path Filters*
15:00-16:00	Speaker: Min Zhang, The Chinese University of Hong Kong (Shenzhen) Title: *Flexible and Stretchable Thin-Film Transistors: From Advanced Materials to Neuromorphic Applications*
16:00-17:00	Speaker: Lining Zhang, Peking University Title: *Accelerating Device Modeling and Design-Technology Co-Optimization with AI Algorithms*
19:00–21:00	Guest Dinner Venue: 四楼龙津房

Conference Agenda

Opening and keynote

Time	Activity
June 10 (Wednesday) 09:00-11:50	Venue：Main Hall, 3F（三楼宴会厅1+2）
Chair: Prof. Ioannis (Yiannis) Vardaxoglou	
09:00-09:05	Opening Ceremony
09:05-09:20	Opening Address
09:20-10:05	Plenary 1：Prof. Dapeng Yu, Academician of the Chinese Academy of Sciences Title: *Everything is Quantizable:Quantum Computing is Everyone’s Responsibility*
10:05-10:20	Coffee Break
10:20-11:05	Plenary 2：Prof. Wei Hong, Academician of the Chinese Academy of Sciences, Southeast University Title: *Research Progress in Terahertz Devices, Chips, and Systems*
11:05-11:50	Plenary 3：Prof. Tianchun Ye, Chinese Academy of Sciences Title: *Technology Innovation in Integrated Circuit Transistor Process*
12:00-13:30	Lunch Buffet Venue: 三楼白鹭轩西餐厅

Conference Agenda

Session 1: Digital and Memory Circuits

Time	Activity
June 10 (Wednesday) 13:30-15:10	Venue: Meeting Room 1, 3F
Chair: Enyi Yao	
13:30-13:50	Invited Speaker 1: Jiang Xu , Hong Kong University of Science and Technology (Guangzhou) Title: *Breaking Interconnect Wall with Electronic-Photonic Integration*
13:50-14:10	Invited Speaker 2: Ye Lu , Fudan University Title: *AI-Empowered Device Compact Model Creation*
14:10-14:25	Oral 1: Longyu Sun, Institute of Microelectronics of the Chinese Academy of Sciences Title: *DTCO for Novel CFET 6N2P 8T-SRAMs with Superior Readability/Writability*
14:25-14:40	Oral 2: Zhenggang Cao, Tianjin University Title: *KPA-Det: Knowledge-Prior-Assisted Pre-Silicon Trust Assessment for Gate-Level Digital Circuits*
14:40-14:55	Oral 3: Man Liu, Tsinghua University Title: *A 65-nm Hardware-Accelerated Secure SoC with Multi-Layer Side-Channel Suppression for Edge Applications*
14:55-15:10	Oral 4: Jingyun Gu, The Hong Kong University of Science and Technology (Guangzhou) Title: *Hardware-Algorithm Co-Design for Digital RRAM-based Computing-in-Memory Accelerators via Outlier-Aware Finetuning*
15:10-15:30	Coffee Break

Conference Agenda

Session 2: ADCs and Power Management Circuits-1

Time	Activity
June 10 (Wednesday) 13:30-15:10	Venue: Meeting Room 2, 3F
Chair: Li Gao	
13:30-13:50	Invited Speaker 1: Cheng Zhuo, Zhejiang University Title: *AI-Driven Virtual Fabrication for ICs*
13:50-14:10	Invited Speaker 2: Quan Pan, Southern University of Science and Technology Title: *Low-Power Wireline Optical transceivers for Emerging High-Speed* Communications
14:10-14:25	Oral 1: Binxiong Huang, Peking University Title: *An Energy-Efficient Cyclic SAR ADC using Capacitively Degenerated Dynamic Amplifier*
14:25-14:40	Oral 2: Tingting Wu, Tianjin University Title: *A 16-bit 1-MS/s SAR ADC with Digital Foreground Calibration and High-Precision Comparator*
14:40-14:55	Oral 3: Jiahao Wu, Tsinghua University Title: *A 55.8dB-SNDR 10MS/s SAR ADC with 0.067mm² Active Area in 130-nm CMOS*
14:55-15:10	Oral 4: Jiakun Sun, Tianjin University Title: *A 50-MHz 7.8 ppm/°C Relaxation Oscillator Using Comparator Offset and Delay Cancellation Techniques*
15:10-15:30	Coffee Break

Conference Agenda

Session 3: Nanoelectronics-1

Time	Activity
June 10 (Wednesday) 13:30-15:15	Venue: Meeting Room 3, 3F
Chair: Yuanyuan Shi	
13:30-13:50	Invited Speaker 1: Chao Ma, Xi'an Jiaotong University Title: *Contact-dominated, field-enhanced flexible pressure sensors toward high-performance robotic skin*
13:50-14:10	Invited Speaker 2: Xuefei Li, Huazhong University of Science and Technology Title: *Ballistic transport in p-type WSe_2 transistors*
14:10-14:30	Invited Speaker 3: Donglin Lu, Hunan University Title: *High-density 3D integration based on 2D semiconductors*
14:30-14:45	Oral 1: Jiaqiao Liang, The Chinese University of Hong Kong, Shenzhen Title: *Schottky Barrier Engineering via Field-Modulation in All-CNT Thin Film Transistors*
14:45-15:00	Oral 2: Renchen Yuan, University of Science and Technology of China Title: *Threshold voltage modulation of MoS2 FETs via Mild AlOx Surface Passivation*
15:00-15:15	Oral 3: Xiangcheng Liu, South China University of Technology Title: *Dual-Gate Thin-Film Transistor with Metal-Induced Crystallized InSnZnO Channel*
15:15-15:30	Coffee Break

Conference Agenda

Session 4: Memory Devices and Tech-1

Time	Activity
June 10 (Wednesday) 13:30-15:10	Venue: Multifunction Room , 3F
Chair: Bobo Tian	
13:30-13:50	Invited Speaker 1: Yang Chai, The Hong Kong Polytechnic University Title: *Bioinspired In-Sensor Computing for Artificial Vision*
13:50-14:10	Invited Speaker 2: Mengnan Ke, Yokohama National Univerisy Title: *Understanding Slow Trap Characteristics and Degradation in GeOx/Ge MOS Structures*
14:10-14:25	Oral 1: Meng Liang, South China University of Technology Title: *Mechanism Transition in Low Temperature CVD Growth of Single Crystalline MoS2 for Back-End-of-Line Compatible Transistors*
14:25-14:40	Oral 2: Renhao Xue, The Hong Kong University of Science and Technology (Guangzhou) Title: *Filament-Free, Multi-Level Bulk-Switching RRAM Enabled by Oxygen-Vacancy Redistribution*
14:40-14:55	Oral 3: Mingche Li, Beihang University Title: *An Efficient and High-Accuracy Complementary Series-Connected SOT-MRAM CIM Architecture*
14:55-15:10	Oral 4: Shengmin Hu, The Hong Kong University of Science and Technology Title: *T-CAD Study of Word-Line Gate-Length Scaling in Vertical 3D NAND FLASH*
15:10-15:30	Coffee Break

Conference Agenda

Session 5: Biological and Sensing Circuits and Devices

Time	Activity
June 10 (Wednesday) 15:30-17:10	Venue: Meeting Room 1 , 3F
Chair: Jianwei Zhong	
15:30-15:50	Invited Speaker 1: Chuan Liu, Sun Yat-sen University Title: *Advances in Metal-Oxide Thin-Film Transistors*
15:50-16:10	Invited Speaker 2: Yancong Qiao, Sun Yat-sen University Title: *Flexible Ultra-Thin Physiological Signal Sensor and Thermal-Electric Conversion System*
16:10-16:25	Oral 1: Jiaju Yin, Tsinghua University Title: *Tear-Driven Wireless Smart Contact Lens for Continuous Monitoring of Dry Eye Disease*
16:25-16:40	Oral 2: Jiayi Cui, Tsinghua University Title: *Epidermal Thin-Film Electronics for Imperceptible Detection of Electrooculogram*
16:40-16:55	Oral 3: Zixuan Ma, Tsinghua Shenzhen International Graduate School Title: *A 3.43-μA, 5.14-NEF Chopper-Stabilized Amplifier with a Fast-Settling DC Servo Loop for Bio-Potential Recording*
16:55-17:10	Oral 4: Xiaocheng Wang, South China University of Technology Title: *High-Mobility MO-TFTs-Based Integrated Pressure Sensors for Multinational Language Recognition*
18:30-21:00	Welcome Reception Venue: 三楼宴会厅1

Conference Agenda

Session 6: ADCs and Power Management Circuits-2

Time	Activity
June 10 (Wednesday) 15:30-17:10	Venue: Meeting Room 2 , 3F
Chair: Guangyin Feng	
15:30-15:50	Invited Speaker 1: Yutao Li, Beijing Institute of Technology Title: *Carbon-based Biomimetics Nanoelectronic Devices and Algorithmic Synergy*
15:50-16:10	Invited Speaker 2: Li Gao, South China University of Technology Title: *Millimeter-Wave Wideband/Reconfigurable Power Amplifiers and Low Noise Amplifiers*
16:10-16:25	Oral 1: Zeyu Wu, Harbin Institute of Technology (Shenzhen) Title: *A Compact D-Band Power Amplifier with 16.2-dBm Output Power and 16.4% Peak PAE*
16:25-16:40	Oral 2: Yutong Xie, Xi'an Jiaotong University Title: *Digital Post-Compensation for Nonlinear Distortion in Broadband Receivers Based on DNN*
16:40-16:55	Oral 3: Ziyun Wu, South China University of Technology Title: *A 100Gb/s Low Power PAM-4 Wireline Receiver Analog Front-End with 15dB Loss Compensation*
16:55-17:10	Oral 4: Zhe Deng, South China University of Technology Title: *A 5.48 ppm/°C VCO with Temperature Compensator in 22nm CMOS*
18:30-21:00	Welcome Reception Venue: 三楼宴会厅1

Conference Agenda

Session 7: Power Devices-1

Time	Activity
June 10 (Wednesday) 15:30-17:25	Venue: Meeting Room 2 , 3F
Chair: Chao Ma	
15:30-15:50	Invited Speaker 1: Ming Qiao, University of Electronic Science and Technology of China Title: *Customized Design of Low-Voltage LDMOS to Reduce Energy Losses for xPU Power Supply*
15:50-16:10	Invited Speaker 2: Zhihong Liu, Xidian University Title: *Progress of GaN-on-Si RF Devices*
16:10-16:25	Oral 1: Xin Wang, Tiangong University Title: *A High-Voltage GaN-Based Class-D Power Amplifier with 300 Vpp Output for 5 kHz–220 kHz Wideband Acoustic Applications*
16:25-16:40	Oral 2: Teng Li, Peking University Title: *Decoupling of Vth and Ion in GaN p-Channel Transistors via Level Shifting Gate Drive Method*
16:40-16:55	Oral 3: Zirui Zhou, South China University of Technology Title: *Optimization of Ti/Al/Ni/Au Ohmic Contacts on AlN/GaN Heterostructures: The Role of in-situ SiN Layer and Ti/Al Thickness Ratio*
16:55-17:10	Oral 4: Tengyu Liu, Xi'an Jiaotong University Title: *Negative-Current-Induced Substrate Electron Injection in Deep N-Well-Isolated GGNMOS*
17:10-17:25	Oral 5: Bo Yi, University of Electronic Science and Technology of China Title: *An E-mode β-Ga2O3 Vertical Fin-MISFET With p-NiO Shield Exhibiting a Breakdown Voltage of 2.9 kV and Power Figure of Merit of 3.8 GWcm2*
18:30-21:00	Welcome Reception Venue: 三楼宴会厅1

Conference Agenda

Session 8: Memory Devices and Tech-2

Time	Activity
June 10 (Wednesday) 15:30-17:10	Venue: Multifunction Room, 3F
Chair: Mengnan Ke	
15:30-15:50	Invited Speaker 1: Bobo Tian, East China Normal University Title: *Ferroelectric devices for in-memory computing*
15:50-16:10	Invited Speaker 2: Yuanyuan Shi, University of Science and Technology of China Title: *2D-semiconductor transistors for advanced logic and memory devices: from channel deposition to device integration*
16:10-16:25	Oral 1: Qiuhong Wang, Xidian University Title: *Three-Dimensional Inversion-Type Ferroelectric Memcapacitors: Physics and Optimization*
16:25-16:40	Oral 2: Xinyu Zou, East China Normal University Title: *Improved SC-RFET for Complete Two-Input Logic-in-Memory Implementation*
16:40-16:55	Oral 3: Jingbo Zhou, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences Title: *Enhanced Thermal Stability of Nanoscale Phase Change Memory Materials by SiN Capping Layer*
16:55-17:10	Oral 4: Haorong Li, Tsinghua University Title: *Tri-State Ferroelectric Transistor Enabled by Electrostatic Coupling*
17:10-17:25	Oral 5: Tianze Yu, Beijing Institute of Technology Title: *Design of Floating-Gate Field-Effect Transistors based on Ferroelectric-Assisted Tunneling*
18:30-21:00	Welcome Reception Venue: 三楼宴会厅1

Conference Agenda

FET 100

Time	Activity
June 11 (Thursday) 09:00-11:15 Venue：Multifunction Room, 3F	
Chair: Mansun Chan	
09:00-09:30	Speaker: Prof. Tian-Ling Ren, Tsinghua University Title: *Novel Device and Chip Technologies Driving Moore's Law*
09:30-10:00	Speaker: Prof. Pui-In Mak, University of Macau Title: *The Frontiers of Microelectronic Engineering over the Next Decade*
10:00-10:30	Speaker: Prof. Han Wang, University of Hong Kong Title: *CMOS Technology in the Nanoscale Era*
10:30-11:00	Panel Discussion
11:00-11:15	Interaction Session: Quiz for prizes
11:15-12:15	Poster Session 1 Venue: 待定
12:15-13:30	Lunch Buffet Venue: 三楼白鹭轩西餐厅

Conference Agenda

Session 9: Analog and Communication Circuits

Time	Activity
June 11 (Thursday) 13:30-15:10	Venue: Meeting Room 1, 3F
Chair: Chunlei Wu	
13:30-13:50	Invited Speaker 1: Jiewei Chen, South China Normal University Title: *Bioinspired Neuromorphic Devices for Broadband Dynamic Information Encoding and Recognition*
13:50-14:05	Oral 1: Xi Deng, School of Integrated Circuits, Huazhong University of Science and Technology Title: *Toward A Tri-Mode AOT Buck Converter With Fast Wake-Up and Direction-Aware On-Time Boosting for AVS Digital Systems*
14:05-14:20	Oral 2: Minhao Wang, Tianjing University Title: *Design of LED Driver Circuit for Light Intensity Compensation in Reflective Optical Encoders*
14:20-14:35	Oral 3: Siyuan Chen, Southern University of Science and Technology Title: *A 12V-Input 1V–1.8V-Output 96.1% Peak Efficiency Dual-Path Flying Capacitor Cross-Connected (DP-CCC) Buck Converter*
14:35-14:55	Coffee Break

Conference Agenda

Session 10 : RF and Microwave Circuits and Devices-1

Time	Activity
June 11 (Thursday) 13:30-14:35	Venue: Meeting Room 2, 3F
Chair: Xiang Yi	
13:30-13:50	Invited Speaker 1: Mohammad Samizadeh Nikoo, Nanyang Technological University Title: *High-Performance Electronic Metadevices for Millimeter-Wave and Terahertz Integrated Circuits*
13:50-14:05	Oral 1: Xinnan Guo, South China University of Technology Title: *A Dual-Core Dual-Mode VCO Using Switch-less Transformer Loop Mode-Switching Technique Achieving 192.7dBc/Hz FoM at 1 MHz offset*
14:05-14:20	Oral 2: Junming Zhu, South China University of Technology Title: *24–33 GHz LC Drain-Source Feedback High- Linearity Doherty Power Amplifier*
14:20-14:35	Oral 3: Haochuan Qiu, South China University of Technology Title: *A Broadband Class-F RF Power Amplifier with 32% PAE and 39.8-dBm Psat for 5G Handset Applications*
14:35-14:55	Coffee Break

Conference Agenda

Session 11: Integrated Silicon Photonics and High-Performance Photodetectors

Time	Activity
June 11 (Thursday) 13:30-15:25	Venue: Meeting Room 3, 3F
Chair: Daquan Zhang	
13:30-13:50	Invited Speaker 1: Eleni Makarona, Institute of Nanoscience and Nanotechnology, NCSR "Demokritos" Title: *Scalable Functional Devices Based on Chemically Synthesized ZnO Nanostructures: Bridging Synthesis and Device Functionality*
13:50-14:10	Invited Speaker 2: Daquan Zhang, The Chinese University of Hong Kong, Shenzhen Title: *Metal halide perovskite nanowire arrays for high-performance optoelectronic devices*
14:10-14:25	Oral 1: Sihan Li, Southern University of Science and Technology Title: *Wavelength Stabilization of a Silicon-Photonic Microring Modulator with Drop-Port-Based Thermal Control Loop in 28-nm CMOS*
14:25-14:40	Oral 2: Guanru Chen, South China University of Technology Title: *InGaAs APD Lifetime Prediction and Reliability Assessment Based on Dark Current Degradation Characteristics*
14:40-14:55	Oral 3: Yuanye Sun, South China University of Technology Title: *High-SNR Micro-Photodetector Integrated with a Broadband Achromatic Metalens*
14:55-15:10	Oral 4: Muhammad Sulaman, Minzu University of China Title: *Interface-Engineered Self-Powered Infrared Photodetectors Based on Surface-Passivated PbSe Quantum Dot Bulk-Heterojunctions*
15:10-15:25	Oral 5: Xinlei Chen, Tianjin University Title: *Influence of implantation and operating temperature on pinning voltage in CIS pixels*
15:25-15:45	Coffee Break

Conference Agenda

Session 12: Wide-Bandgap Semiconductors: Contacts, Devices, and Reliability

Time	Activity
June 11 (Thursday) 13:30-14:55	Venue: Multifunction Room , 3F
Chair: Huaxing Jiang	
13:30-13:50	Invited Speaker 1: Sunbin Deng, Huazhong University of Science and Technology Title: *BEOL-Compatible Oxide Power Transistors for On-Chip Active Power Delivery Networks in 3D ICs*
13:50-14:10	Invited Speaker 2: Dexing Liu, The Chinese University of Hong Kong, Shenzhen Title: *Making Efficient Electrical Contacts in Low-Dimensional Semiconductors*
14:10-14:25	Oral 1: Haoran Zhang, Xidian University Title: *High-Temperature Reconfigurable AlSc0.4N-Gated AlGaN/GaN HEMTs with Wide Vth Tunability*
14:25-14:40	Oral 2: Shiqing Qin, Southeast University Title: *Reliability of GaN HEMT-Investigation on HTRB-induced degradations for GaN GIT bidirectional device*
14:40-14:55	Oral 3: Zikang Wu, Sun Yat-sen University Title: *A 5.8 GHz 86 fs-rms Jitter DPLL With Low Noise TVC and Noise Shaping SAR ADC*
14:55-15:15	Coffee Break

Conference Agenda

Session 13: Emerging Sensors and Neuromorphic Devices

Time	Activity
June 11 (Thursday) 15:10-16:10	Venue: Meeting Room 1 , 3F
Chair: Jiewei Chen	
15:10-15:25	Oral 1: Junju Huang, The Hong Kong University of Science and Technology (Guangzhou) Title: *A High Dynamic Range Flip-Chop Analog Counter with Feedback Charge Injection for SPAD Sensors*
15:25-15:40	Oral 2: Qiaoqiao Kang, Tsinghua University Title: *Modelling of A Novel MEMS Microphone with Lumped Parameters*
15:40-15:55	Oral 3: Xiao He, Huazhong University of Science and Technology Title: *A High-Performance 1T1F Volatile DRAM Architecture Based on 2D MoS_2 for Neuromorphic Computing*
15:55-16:10	Oral 4: Xianyu Wang, Peking University Title: *A Differential Memcapacitor-based Synaptic Circuit for Robust Spiking Neural Network Inference*
16:30–17:30	POSTER Session 2/Lab Tour to SCUT
18:30-21:00	Dinner Buffet Venue: 三楼白鹭轩西餐厅

Conference Agenda

Session 14 : RF and Microwave Circuits and Devices-2

Time	Activity
June 11 (Thursday) 15:10-16:35	Venue: Meeting Room 2 , 3F
Chair: Eleni Makarona	
15:10-15:30	Invited Speaker 1: Chunlei Wu, Fudan University Title: *Physical Modeling of the Subthreshold Swing Saturation Behavior in Cryogenic MOSFETs*
15:30-15:50	Invited Speaker 2: Jing Ming, TuoTuo Technology (Suzhou) Co., Ltd. Title: *Rapid Manufacturing of Metamaterial Microwave Devices via Lithography*
15:50-16:05	Oral 1: Chang Liu, The Hong Kong University of Science and Technology (Guangzhou) Title: *A Missing-Code Free Ring Oscillator TDC through Digital Calibrations*
16:05-16:20	Oral 2: Ziwei Jin, The Chinese University of Hong Kong Title: *A Split Noise-Coupled Multi-Cell Linear_Exponential Incremental ADC*
16:20-16:35	Oral 3: Runkun Li, The Chinese University of Hong Kong Title: *A Dual-Band Bandpass Delta-Sigma Modulator with Capacitor-Reused Eight-Path Filters*
16:35–17:30	POSTER Session 2/Lab Tour to SCUT
18:30-21:00	Dinner Buffet Venue: 三楼白鹭轩西餐厅

Conference Agenda

Session 15: Nanoelectronics

Time	Activity
June 11 (Thursday) 15:45-17:10	Venue: Meeting Room 3 , 3F
Chair: Dexing Liu	
15:45-16:05	Invited Speaker 1: Qianqian Huang, Peking University Title: *Si Hybrid Tunnel FET-CMOS Foundry Platform for Ultra-low-Power Circuit Applications*
16:05-16:25	Invited Speaker 2: Qiming Shao, Hong Kong University of Science and Technology Title: *Scaling probabilistic computing for AI and optimization*
16:25-16:40	Oral 1: Fangxing Zhang, Peking University Title: *New Insights into the Channel Charge and Terminal Partition of Si-TFETs: Physics and Modeling Methods*
16:40-16:55	Oral 2: Jiaquan Fang, Hong Kong University of Science and Technology Title: *A Physics-Informed HyperNetwork Compact Model for 2D-FETs with Geometry and Process Adaptability*
16:55-17:10	Oral 3: Lutong Wang, Peking University Title: *3D Stacked Inverter Based on Ge/Al and InAlZnO Complementary Thin-Film Transistors*
17:10–18:10	POSTER Session 2/Lab Tour to SCUT
18:30-21:00	Dinner Buffet Venue: 三楼白鹭轩西餐厅

Conference Agenda

Session 16: Process Design and Device Modeling

Time	Activity
June 11 (Thursday) 15:15-15:50	Venue: Multifunction Room, 3F
Chair: Sunbin Deng	
15:15-15:35	Invited Speaker 1: Cher Ming Tan, Chang Gung University Title: *A Multi-Physics Toolkit for Predictive Electromigration Modeling in Advanced IC Interconnections*
15:35-15:50	Oral 1: Shuaihong Li, Tsinghua University Title: *TCAD Simulation of GIDL Suppression in Junctionless Vertical Channel Transistor (VCT)*
16:30–17:30	POSTER Session 2/Lab Tour to SCUT
18:30-21:00	Dinner Buffet Venue: 三楼白鹭轩西餐厅

Conference Agenda

Session 17: Device Reliability

Time	Activity
June 12 (Friday) 09:00-10:40	Venue: Meeting Room 1, 3F
Chair: Zichao Ma	
09:00-09:20	Invited Speaker 1: Yeliang Wang, Beijing Institute of Technology Title: *Tunning Properties of Novel 2D Heterostructures & Devices*
09:20-09:40	Invited Speaker 2: Jiuren Zhou, Xidian University Title: *>10^{10}-Cycle Endurance in Wurtzite Ferroelectrics via a Superlattice and Recovery Protocol Enabling Vacancy Confinement*
09:40-09:55	Oral 1: Zhengjun Hu, Chinese Academy of Sciences Title: *Influential Mechanism of Dual-Temperature SiO2 Passivation on IGZO Transistor Reliability*
09:55-10:10	Oral 2: Yansheng Zhao, Peking University Title: *Hot Carrier Generation and Transport in MoS2 FETs: An Ensemble Monte Carlo Simulation Study*
10:10-10:25	Oral 3: Yijun Shi, China Electronic Product Reliability and Environmental Testing Research Institute Title: *Temperature-Dependent ESD Robustness of Schottky-Gate p-GaN HEMTs*
10:25-10:40	Oral 4: Shaoxin Yu, Runpeng Semiconductor Technology Title: *An Effective Copper BEOL Solution in Sub-90nm HV BCD Circuits*
10:40-11:00	Coffee Break

Conference Agenda

Session 18: EDA And AI-1

Time	Activity
June 12 (Friday) 09:00-10:05	Venue: Multifunction Room, 3F
Chair: Changjian Zhou	
09:00-09:20	Invited Speaker 1: Kanhao Xue, Huazhong University of Science and Technology Title: *On the direct bandgap of GaN and indirect bandgap of GaP*
09:20-09:35	Oral 1: Yiwei Zhang, Tsinghua University Title: *Data-Efficient Multi-Objective Design of RF PiN Diodes via Active Learning*
09:35-09:50	Oral 2: Muyuan Peng, The University of Hong Kong Title: *HIMSA: A Heterogeneous In-Memory Computing and Searching Architecture for Efficient Attention-Based Models*
09:50-10:05	Oral 3: Yanxu Ji, National University of Defense Technology Title: *Toward Hardware-Friendly Invertible Logic: A Linear Programming Approach for P-Bit Network*
10:05-10:25	Coffee Break

Conference Agenda

Session 19: Display and Imager

Time	Activity
June 12 (Friday) 11:00-11:45	Venue: Meeting Room 1, 3F
Chair:Jiuren Zhou	
11:00-11:15	Oral 1: Hongzhao Wu, ZJU-Hangzhou Global Scientific and Technological Innovation Centre Title: *Gate-programmable spectral responsivity in photodetector for filter-less color perception*
11:15-11:30	Oral 2: Weiming Yuan, Peking University Title: *A Resolution-Preserving 2×2 Rolling-Binning Active Pixel Sensor for Low-Dose X-Ray Imaging*
11:30-11:45	Oral 3: Shuai Shen, Guangdong Baiyun University Title: *A Bidirectional Gate Driver Circuit with Cascaded Two-Stage Pre-Charge for In-Cell Touch Panels*
12:00-13:00	Lunch Buffet Venue: 三楼白鹭轩西餐厅

Conference Agenda

Session 20: EDA And AI-2

Time	Activity
June 12 (Friday) 10:25–11:25	Venue: Multifunction Room, 3F
Chair: Kanhao Xue	
10:25-10:40	Oral 1: Wendi Xu, Southeast University Title: *Generative inverse design of fabrication-aware freeform nanophotonics via unsupervised learning*
10:40-10:55	Oral 2: Huanhuan Zeng,Tsinghua University Title: *A Data-Efficient Inverse Design Framework for 4HSiC MOSFETs Via Active Learning and High-Dimensional Multi-Objective Optimization*
10:55-11:10	Oral 3: Yi Wang, Huazhong University of Science and Technology Title: *A Hardware-Algorithm Co-Design for High-Throughput SNN Training via Layer-Wise In-Situ Updates on Systolic Arrays*
11:10-11:25	Oral 4: Mengge Jin, East China Normal University Title: *An ASAP7-Compatible Reconfigurable Field-Effect Transistor (RFET) PDK Enabling Post-Layout Verification of Reconfigurable Logic*
12:00-13:00	Lunch Buffet Venue: 三楼白鹭轩西餐厅

Poster Session 1

No.	Name	Title
June 11 (Thursday) 11:15-12:15		**Venue: Multifunction Room, 3F**
1	Shuyu Mo	A 9-12b 1-6MS/s Reconfigurable SAR ADC with a Split-FIA Comparator and Binary-Recombination-Redundancy CDAC
2	Qing He Wang	Strength of remote phonon scattering in metal-gate thin-film transistors with high-k gate dielectric
3	Jiaying He	Effect of Ar/O_2 Ratios on the Performance and Stability of ITWO Thin Film Transistors by the RF Sputtering method
4	Xiyue Li	The Effects of Higher-order subbands on the Hole Mobility Gain of Wurtzite GaN/AlN Quantum well
5	Zhiqi Li	A Transformer-based Architecture Exploration Framework for Routerless NoC
6	Hao Wang	Solving Circuit Partitioning Based on Ising Model Mapping and High-Order Reduction
7	Boyu Luo	A Fully CMOS Low-Power Bandgap Reference Circuit with Segmented Compensation Structure
8	Junxiang Wen	Design of a 4th-order Multi-stage Wideband High Gain Feedforward Operational Amplifier
9	Jing Li	A Low-Noise and High-Linearity Analog Front-End ASIC for High-Resolution Radiation Detectors
10	Bin Hu	A High-Linearity 0.1-6 GHz RF Receiver with 13.8 dBm In-Band IIP3 in 22 nm CMOS
11	Ruqiu CHEN	A 12bit 10MSPS SAR ADC Using Reference Ripple Cancellation to Achieve 70.01 dB SNDR
12	Zhenyu Chen	A 120MHz-BW 73.41dB-SNDR Continuous-Time Sigma-Delta Modulator with a 4.915-GHz Sampling Clock for Communication Systems
13	YanhuiSong	A High-Efficiency, Low-Latency Polynomial Multiplication Accelerator for Lattice-based Cryptosystems
14	Lang Qin	Efficient Zero-Skipping Transposed Convolution for In-Memory Image Decompression
15	Longbiao Liu	A Fast Transient Response LDO with High PSR Using Three-Stage Parallel Enhanced SSF
16	Huizhe Pang	A Wide Range Variable Slope Digital to Time Converter with Linearity Enhancement for Radar Applications
17	Tao Liu	A CMOS W-Band Frequency Quadrupler with Asymmetric Transformer Balun for High Harmonic Rejection
18	Jiahao Zhou	A CMOS MmW Low Phase Error Variable Gain Low Noise Amplifier for 5G NR FR2 Band Receivers
19	Qiuwen Zeng	A D-Band High-Linearity Passive Mixer with 7.7dBm IP1dB and 18.9dBm IIP3 in 65nm CMOS
20	Jiayu Chen	A High-Gain Driver Amplifier Operating from 0.05 to 3 GHz Using a Darlington Transistor and Feedback Configuration
21	Dujie He	A Low Power Series-Parallel Resonace VCO With Single Resonant Frequency
22	Geen Hu	A 27-31 GHz 6-bit Phase Shifter with 9.32 dBm IP1dB and 2.2° RMS Phase Error in 28-nm CMOS
23	Tao Su	Design of a 24GHz SIW Filter Based on Hybrid Coupling Structure
24	Jiayu Chen	A 2-18GHz Non-uniform Distributed Ultra-wideband Power Amplifier
25	Zhaonian Yang	Improved High-Holding Voltage ESD Protection MOSFET Device With Drain-Side Engineering

Poster Session 1

No.	Name	Title
June 11 (Thursday) 11:15-12:15		**Venue: Multifunction Room, 3F**
26	Chenxu Niu	Reliability Study on Thickness and Area Dependent TDDB Characteristics of Hafnium-based Oxide Capacitors
27	HinCheung Yu	GAAFETs Reliability Using Four-States Model for Si/SiO2/High-K Interface in TCAD Simulation
28	Sihao Wu	Photosensitive p-type Ge/Al Thin-Film Transistors for Image Sensor Applications
29	Wenjuan Zhou	A Compact Augmented Resistive Crossbar for Solving Linear Systems
30	Xiaohan Meng	3D-Stacked MoS_2 /IGZO Heterogeneous Flash Memory for High-Density Storage
31	Yuhao Zhou	Energy-Efficient Logic-in-Memory Computing Enabled by Double-Gated Feedback Charge-Trapping Memory
32	Tingrui Huang	High-Voltage InSnO Ferroelectric Metal Field-Effect Transistor with Tunable On-Resistance and Breakdown Voltage
33	Qiming Zhao	An Integrated Broadband Hybrid Architecture CMOS Magnetic Sensor for Power IoT Application
34	Bingyan Pang	Comparative Thermal Analysis and Compact Thermal Modeling of Backside Power Delivery in GAAFETs
35	Baisen Liu	High-power GaN-based blue laser diode COS package simulation and optimization design
36	Minghao Liang	Coupled Degradation Behaviors in Monolithically Integrated GaN Power Chips Under Repetitive ESD Stress
37	Chaozheng Qin	Fast Cell Library Characterization based on Transfer Learning
38	Zhou Fanjie	Hardware-Friendly Full-Integer Quantization and FPGA Acceleration for Vision Transformers
39	Yisong Zhao	Design of a Wide-Input-Range High-Side Pre-Driver for ASIL-D Automotive Applications
40	Rongxing Qin	A 0.85–1.55 GHz Low-Power Ring Oscillator with Enhanced Tuning Linearity
41	YaoXu An	A Charge-Domain Convolution Amplifier for Centroid Calculation in Infrared Readout Circuits
42	Jiale Liu	Label-Free Detection of miRNA 106a Using TDN Functionalized Extended Gate ITZO Thin-Film Transistor Biosensor
43	Haolong Lin	A 6-Gb/s Wireline Receiver Analog Front End with Hybrid Equalizer for 28-dB Loss Compensation
44	Hongli He	Recent Advances in Multi-Functional Reconfigurable Intelligent Surfaces: A CMOS-Empowered Perspective for 6G and Beyond
45	Hongbo Chen	A 177.1-dB-FoMs Stage-Interleaved Op-Amp-Reuse CIFB ΔΣ ADC with 15.2 μW Power Consumption
46	Ruhui Guo	A Power-Efficient Hybrid ADC combining Single-Slope ADC and Continuous-Time Sigma-Delta Modulator
47	Zhongze Liu	An 80-MHz BW 60-dB SNDR Bandpass Time-Interleaved Noise Shaping SAR ADC with Passive Residue Summation
48	Ruiqi Song	A 14-ENOB Second-Order Passive Noise-Shaping SAR ADC With DAC Mismatch Error Shaping
49	sheng huang	An 18bit 80MS/s Cyclic ADC with 84dB SNDR in 55nm CMOS
50	Xiangmin Yang	A 16-Bit 50-MS/s SAR ADC with Multi-Bit Per Cycle Quantization

Poster Session 2

No.	Name	Title
June 11（Thursday）11:15-12:15 Venue: Multifunction Room, 3F		
51	Aoshen Zhao	An Energy-Efficient and High-Dynamic-Range Two-Step ΔΣ ADC for CMOS Imager Sensor
52	Zihao Li	A 12 bit 100 MS/s SAR-Assisted Digital-Slope ADC in 40 nm CMOS Technology with 62.57 dB SNDR
53	Xiaohan Zhu	A Configurable HOG-LE Stereo Matching Accelerator for Endoscopic Applications
54	HaijinZhang	Low-Overhead Hardware Error Detection for PE Arrays via Arithmetic Residue Codes
55	Zhuoxuan Wu	A Hardware-Efficient SEC-DAEC ECC Scheme for MBU-Tolerant in Processor
56	Junyi Huang	Adaptive Multi-Gain Miller Compensation for False Turn-On in All-GaN Buck Converters
57	Chengcheng An	A 22-28/33-45 GHz Reconfigurable Dual-Band Phase Shifter in 28-nm bulk CMOS for 5G Application
58	Runpeng Zhang	A 30-MHz, 150-W High-Efficiency GaN Class-E RF Solid-State Power Source for Medical Cyclotrons
59	Liu Yang	Parasitic Analysis and Structural Optimization of GSG Pads for 80-GHz RF Characterization
60	zhencheng xu	A 1.97-GHz AlN BAW Filter With Performance Enhancement Using Active Negative Capacitors
61	Xiaoqing Liu	Study on Passivation Layer Cracking in High-Precision Analog Chip Manufacturing
62	Lu Chang	A Dual-Data Programming AMOLED Pixel Circuit with highly Widen Data Voltage Range
63	Haorong Li	Fabrication of Perovskite-Based Solar Cell for Self-Powered Smart Contact Lenses
64	Jiahao Chen	Comparison of DC and RF Magnetron Sputtered NiOx for Perovskite Solar mini-module
65	Sheng Jiang	A Reconfigurable MPUF With Thermal Noise Based SOT-MRAM
66	Weimeng Zhao	Low-Power Complementary VGSOT-MRAM with Hierarchical Architecture and Enhanced Sensing
67	Zijia Su	Floating-Gate Coupled FET Unit for Nonvolatile and Multifunctional Electronic Devices
68	Di Wu	A Bidirectional 2T2F FeFET TCAM Cell for In-Array Search and Hamming distance Computing
69	Tianzi Gao	A Capacitance-Coupling-Based Test for the Hidden Open Defects in 2T0C DRAM
70	Haiyu Xie	A Flexible TFT-Based Pressure Sensing System for Physiological Waveform Monitoring
71	Yifan Li	A Dual-Radius Sector Piezoelectric Micromachined Ultrasonic Transducer
72	Ali Imran	Solar Blind Photodetector based on Bulk LiNbO3
73	Yansong Wang	A Robust Current-Mode Gray-Code Readout Chain for Optical Encoder Chips
74	Xintong Wang	MemGate-SNN: Membrane-Potential Confidence Gating for Energy-Efficient Spiking Neural Networks
75	Zifan Li	A Dynamic Mixed Gas Concentration Identification Method Using Spiking Reservoir Computing
76	Yu Long	An Analog Front-End Circuit for MEMS Thermal Flow Sensors
77	Chen Chen	Cascaded Pancharatnam-Berry Metasurfaces for High-Resolution Transverse Displacement Sensing in the Visible Regime

Poster Session 2

No.	Name	Title
June 11（Thursday）16:30-17:30 Venue: Multifunction Room, 3F		
78	Jian Hu	Leakage Current Degradation Behavior and Mechanism Analysis of 1200V SiC Power MOSFETs Under Repetitive Surge Current Stress
79	Chengju Zhou	Impact of Field Plate Structure on the Capacitance Characteristics of GaN based HEMT Power Devices
80	Ping Ding	Hardware-Software Co-optimization for Chiplet-Based Edge Machine Learning Acceleration
81	Kunpeng Wang	An efficient approach for MTJ device modeling based on deep neural networks
82	Pengxin Zhou	Study on Degradation Characteristics of SiC Power MOSFETs under High-Frequency Gate Switching Stress
83	Yuxin Zhang	Frequency Spectrum Analysis of Passive Intermodulation Under Broadband Excitation
84	Minhao Wang	Design of an Absolute Optical Encoder Sensor Chip with Low Absolute-Code Duty-Cycle Deviation
85	Haifeng Wu	Process evaluation for MoS2 based GAAFETs
86	Yongli Lin	A High-SNR Fluorescence Detector Based on Photodiode Body-biased MOSFET for qPCR
87	Zhanxiong Qiu	Enhanced Photoresponse via Interlayer Gating in WSe_2/Graphene/InSe Heterojunction Photodetectors
88	YadingYi	Forming Polarity Dependent Threshold Voltage Asymmetry in Ag/HfO_2/Ag Volatile Memristors
89	Yanfeng Wu	Study on High-Temperature Aging Effects and Failure Mechanisms of MEMS Pressure Sensors
90	Shubo Zhang	Infrared Image Enhancement Based on Dual-Layer Guided Filtering and FPGA Implementation
91	Yubin Peng	10-MHz-to-67-GHz AlN On-Carrier Differential Matching Network for Electro-Absorption Modulator Drivers
92	Fangyu Zhou	Effect of Rapid Thermal Annealing on High-k Dielectrics
93	Yijiang Liu	1.2-kV Rectangular SiC MOSFET with P-well Layout Modification for Optimal Balance of Conduction, Switching, and Reliability
94	Hongbo Chen	A Hardware-Efficient High-Linearity Multi-Bit Delta-Sigma Modulator Using an Inner DSM Quantizer and a Single-Bit CDAC
95	Song Tang	PyTorch-Based Modeling of p-Type Organic TFT Using Gradient Descent Optimization
96	Luchuan Xu	A dB-Linear Digitally Programmable Analog Baseband for W-Band Radar Applications
97	Aguan Hong	Recent Advances in Silicon-Based Ultra-Wideband Radar Chipsets
98	Zhiyuan Wang	Photocarrier-Induced Field Inversion and Reconfigurable Rectification in MoS_2/WSe_2 Vertical Heterostructures
99	Xinlong Huang	Fracture Strength and Mechanism Analysis of MEMS Cantilever Beams
100	Ruizhe Kuang	A 72 Gb/s PAM-4 Analog Front End System in 65nm CMOS
101	Tian Yu	Deep Learning-Enhanced Ka-Band VCO with Optimized Inductive Tuning
102	DankeChen	AReconfigurable Optoelectronic Device with Mixed-Dimensional Heterojunctions for Efficient Visual Signal Processing

Invited Speakers

Invited Speakers-Tutorial

Kong-Pang Pun

The Chinese University of Hong Kong, China

Biography

Prof. Kong-pang Pun received his B.Eng. and M.Phil. degrees in Electronic Engineering from the Chinese University of Hong Kong (CUHK) and his Ph.D. degree in Electrical and Computer Engineering from the Instituto Superior Técnico, University of Lisbon, Portugal. He is currently a full professor in the Department of Electronic Engineering at CUHK. Prof. Pun was the General Co-Chair and Technical Program co-chair of the IEEE EDSSC in 2008 and 2016, respectively, among his other services.

Prof. Pun's expertise includes high power-efficiency integrated circuits for data conversion and natural signal interface. He has published over 200 peer-reviewed journal and conference papers and co-authored two books in the area of CMOS integrated circuits design. He pioneered the field of N-path filter-based bandpass Delta-Sigma modulators.

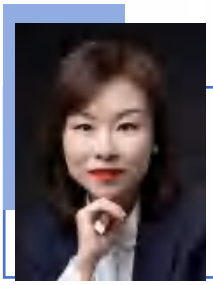
Speech Title

Design of Bandpass Delta-Sigma Modulators Based on N-path Filters

Abstract

Bandpass delta-sigma modulators (BP-DSMs) are specialized analog-to-digital converters (ADCs) designed to digitize narrowband signals centered at high frequencies, such as intermediate or radio frequencies. They find unique applications in digital radio receivers, software-defined radio, radar and sonar systems, and medical ultrasound imaging by offering critical benefits like the elimination of analog mixers, exceptional narrowband resolution, and frequency programmability. Traditionally, BP-DSM loop filters are implemented using active-RC, Gm-LC, or Gm-C circuits. However, as power efficiency and integration demands increase, a new class of BP-DSMs based on switched-RC N-path filters (NPFs) has emerged. Compared to conventional approaches, NPF-based BP-DSMs offer better compatibility with advanced CMOS processes, superior power efficiency, and wider center-frequency programmability for narrowband signals. This tutorial will walk attendees through the architectural design and practical circuit implementation of the NPF-based BP-DSM with design examples, concluding with a perspective on the future of this technology.

Invited Speakers-Tutorial



Min Zhang

The Chinese University of Hong Kong, Shenzhen, China

Biography

Min Zhang is a Professor and Presidential Fellow of the School of Science and Engineering at the Chinese University of Hong Kong, Shenzhen. She received her bachelor and master degrees from Xi'an Jiaotong University and her Ph.D. degree from the Department of Electronic and Computer Engineering at Hong Kong University of Science and Technology. She held academic and industrial positions at Solomon Systech Limited (Hong Kong), Peking University, and Hong Kong Applied Science and Technology Research Institute from 2006 to 2024. Her research interests focus on emerging microelectronic devices, including flexible and stretchable electronics, neuromorphic electronics, nanoelectronics, bioelectronics, and advanced displays. She has published over 160 peer-reviewed papers and 4 book chapters, and has been authorized with more than 20 patents. She has been invited to deliver tutorials and invited talks at more than 30 renowned international conferences. She is a senior member of IEEE, an associate editor of IEEE Open Journal on Immersive Displays, a technical committee member of SID Beijing Branch. She has served as technical program chairs/committees and organizing chairs/committees in numerous conferences, and reviewers for numerous prestigious journals.

Speech Title

Flexible and stretchable thin-film transistors: From Advanced Materials to Neuromorphic Applications

Abstract

Flexible and stretchable electronics have garnered intense interest due to their transformative potential for emerging applications, ranging from imperceptible wearable devices and skin prosthesis repair to soft robotic perceptions and conformable human-machine interfaces. However, the field continues to face challenging obstacles, including material self-limiting fabrication, the trade-off between mechanical flexibility and electrical performance, and the need for stable large-area integration. Nanocarbon based electronics is of great promise to solve these problems for their intrinsic flexibility or stretchability, high carrier mobility, and capability to synthesize as semiconducting or metallic. At the same time, the landscape of flexible thin-film transistors (TFTs) has significantly expanded to include high-performance metal oxide semiconductors, specifically Indium Gallium Zinc Oxide (IGZO), and flexible silicon technologies. These materials provide complementary advantages in terms of CMOS, mobility, uniformity, and compatibility with established fabrication processes.

Beyond logic and control circuits, a pivotal frontier in this domain is the development of TFT-based synaptic transistors, which mimic biological plasticity to enable hardware-level neuromorphic computing and artificial intelligence at the edge. This tutorial will provide a comprehensive overview of the state-of-the-art in flexible and stretchable TFTs. We will examine the device physics, fabrication mechanisms, and circuit integration of carbon nanotube, IGZO, and flexible silicon-based active layers. Special emphasis will be placed on the design and operation of synaptic transistors for neuromorphic applications, as well as strategies for future system integration. By bridging the gap between novel semiconductor materials and bio-inspired computing architectures, this session aims to propose versatile solutions for the next generation of intelligent, soft electronic systems.

Invited Speakers-Tutorial

Lining Zhang

Peking University, China

Biography

Lining Zhang is an Assistant Professor in the School of Electronic and Computer Engineering at Peking University, Shenzhen. He received his Ph.D. from the Hong Kong University of Science and Technology. His research focuses on model-driven next-generation computing systems, advanced electronic design automation (EDA), neuromorphic computing, and novel logic and memory devices.

Speech Title

Accelerating Device Modeling and Design-Technology Co-Optimization with AI Algorithms

Abstract

In the post-Moore era, Design-Technology Co-Optimization (DTCO) is indispensable for meeting advanced power, performance, and area (PPA) requirements. However, traditional physics-based compact models suffer from explosive parameter growth and lengthy development cycles. This tutorial introduces modern Machine Learning-based Device Modeling (MLDM) as an agile and highly accurate alternative. It presents the innovative PHIMO-NN framework, which bridges device physics and artificial neural networks. By embedding tiny neural networks into a physical backbone, PHIMO-NN successfully captures complex short-channel and mobility degradation effects while maintaining strict physical consistency and robust extrapolation capabilities. Fully implemented in Verilog-A, this framework reduces parameter complexity by over 70% and significantly accelerates circuit simulation workflows compared to conventional BSIM models. Finally, the tutorial highlights the open-source Peking University Predictive PDK (PKP), showcasing how it enables standard-cell and end-to-end DTCO pathfinding for advanced nanosheet Gate-All-Around (GAA) architectures.

Invited Speakers-Session 1

Jiang Xu

Hong Kong University of Science and Technology (Guangzhou), China

Biography

Prof. Jiang Xu received his PhD from Princeton University and worked at Bell Labs, NEC Labs, and a startup company which is acquired by Qualcomm. He is the Founding Head of Microelectronics Thrust at Hong Kong University of Science and Technology (Guangzhou). Prof. Xu serves as the Associate Editor for IEEE TCAD and on the steering committees, organizing committees, and technical program committees of many international conferences, including OFC, DAC, DATE, ICCAD, CASES, CODES+ISSS, ASP-DAC, etc. Prof. Xu is awarded IEEE Computer Society Distinguished Contributor as the Charter Member in 2021. He was an IEEE Computer Society Distinguished Visitor and an ACM Distinguished Speaker. He authored and coauthored more than 180 book chapters and papers in peer-reviewed international journals and conferences. Prof. Xu and his students received Special Feature Award from ASP-DAC in 2026, Best Paper Award from the International Symposium on Memory Systems in 2023, IEEE Technical Committee on VLSI Best Paper Award of ISVLSI in 2018, and Best Poster Award from AMD Technical Forum and Exhibition in 2010. His research areas include AI system, electronic-photonic integration, power delivery and management, and hardware/software codesign.

Speech Title

Breaking Interconnect Wall with Electronic-Photonic Integration

Abstract

In the last 15 years, AI applications have required 4.3X more computation capacity every year, while Moore's Law can only offer 1.7X per year. AI systems are relying on not only advanced integration but also aggregation of growing numbers of GPU, CPU, accelerators and memories to meet the burgeoning performance requirements of AI applications under tight cost, energy, thermal, space, and weight constraints. However, interconnect technology develops slower than GPU, CPU and accelerators, and the gap is widening at 1.47X per year. This interconnect wall has become the major bottleneck of AI systems. Electronic-photonic integration piggybacks onto matured fabrication technologies to provide viable solutions to break the interconnect wall. Based on our decade-long quest to transform existing electronic computing systems with photonics, this talk will highlight our recent progress on electronic-photonic integration for aggregated systems.

Invited Speakers-Session 1

Ye Lu

Fudan University, China

Biography

Dr. Ye Lu obtained his Ph.D. from the University of Pennsylvania in 2011, and he had been with Intel and Qualcomm from 2011-2019. Dr. Lu joined Fudan University as a faculty member in early 2020, and his current research interest includes device and design co-optimization (DTCO) and AI-EDA. Dr. Lu is also a co-founder of RFIC-GPT.

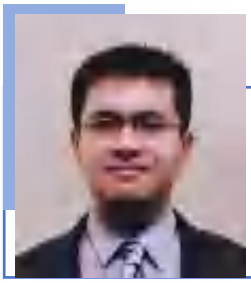
Speech Title

AI-Empowered Device Compact Model Creation

Abstract

Device Compact Model (DCM) is a key bridge between device / process technology and circuit design simulations. Traditionally, DCM is created by physics-based formulas with human extracted parameters, however, this method is labor intensive and time consuming. This talk will cover our recent advancements in creating DCM using AI techniques such as neural networks and symbolic regression. In addition, the methodology of extracting DCM parameters using reinforcement learning (RL) will also be discussed. These results are expected to promote the efficiency as well as accuracy of future DCM development, and facilitate rapid DTCO cycles.

Invited Speakers-Session 2



Cheng Zhuo

Zhejiang University, China

Biography

Dr. Cheng Zhuo is a Qiushi Distinguished Professor at Zhejiang University and Vice Dean of the College of Integrated Circuits. His research interests include VLSI design, electronic design automation (EDA), and AI algorithms and systems. He has published over 200 papers in leading conferences and journals in these areas, earning five Best Paper Awards and seven Best Paper Award nominations. He currently serves or has previously served as an associate editor for journals including IEEE TCAD, ACM TODEAS, and Elsevier Integration, and has served as Chair of the ACM SIGDA East China Chapter. He has also received the First Prize of the Zhejiang Provincial Science and Technology Progress Award and the First Prize of the Zhejiang Provincial Teaching Achievement Award, among other honors.

Speech Title

AI-Driven Virtual Fabrication for ICs

Abstract

Amid steadily increasing process complexity and rapidly rising R&D costs, IC fabrication faces major challenges, including long development cycles and costly trial-and-error. Traditional methodologies and infrastructure struggle to support rapid iteration and fast-paced innovation. AI-driven virtual fabrication is emerging as a promising pathway to accelerate IC R&D and enhance process optimization. This report outlines key research challenges and highlights practical efforts in virtual fabrication for ICs.

Invited Speakers-Session 2

Quan Pan

Southern University of Science and technology, China

Biography

Quan Pan (Senior Member, IEEE) received his B.S degree in Electrical Engineering (EE) at University of Science and Technology of China (USTC) in 2005, and his Ph.D. degree in Electronics and Computer Engineering (ECE) at the Hong Kong University of Science and Technology (HKUST) in 2014.

From 2014 to 2018, he was Senior Staff Engineer in one Silicon Valley startup company, working on 400GbE high-speed SerDes. He joined in the School of Microelectronics, Southern University of Science and Technology as an assistant professor in 2018 and now a tenured full professor. His research interests include High-speed optical transceiver, wireless and wireline circuit design. Dr. Pan has contributed more than 80 peer-reviewed articles. He received the 2017 Outstanding Young Author Award of IEEE Circuits and System Society. He serves as an active reviewer for many international journals, including JSSC, TCAS, TVLSI, JLT, PTL, JoS, and et al.

Speech Title

Low-Power Wireline Optical transceivers for Emerging High-Speed Communications

Abstract

Low-power wireline integrated circuits have become extremely attractive since they are extensively adopted in high-speed communications, such as local area networks, board-to-board, and data center-to-data centers. Energy-efficient 56-224Gbps/lane links with sophisticated equalizations and modulations are studied, including analog front-ends, high-speed drivers, and crosstalk cancellations among multi-channel systems. Moreover, high-speed optical communication ICs have been very charming in recent years, including transimpedance amplifiers, continuous-time linear equalizers, decision feedback equalizers, feedforward equalizers, MZM/VCSEL/DML drivers and clock data recovery circuits.

Invited Speakers-Session 3

Chao Ma

Xi'an Jiaotong University, China

Biography

Dr. Chao Ma is currently an Associate Professor and Ph.D. Supervisor at the School of Microelectronics, Xi'an Jiaotong University, and was selected for the XJTU Young Talent Support Plan. He received his Ph.D. degree in Electrical Engineering from Xi'an Jiaotong University in 2021, during which he was a visiting scholar at the University of California, Los Angeles (UCLA). After graduation, he conducted postdoctoral research at the School of Electronics, Peking University, as a "Boya" Postdoctoral Fellow. His research interests lie in high-performance pressure sensing and low-dimensional device integration, with a focus on: (1) AI-enabled tactile dexterous hands; (2) novel-principle sensing devices and electronic circuits, including (but not limited to) non-Hermitian electronic circuits; and (3) low-dimensional device integration for in-sensor computing. In recent years, he has published papers in leading journals, including Nature Electronics (front cover), Nature Communications, ACS Nano, and IEEE Electron Device Letters. He also holds five granted Chinese invention patents.

Speech Title

Contact-dominated, field-enhanced flexible pressure sensors toward high-performance robotic skin

Abstract

Motivated by the vision of functionalizing diverse human orientated future intelligent technologies with the ability to accurately and robustly detect various mechanical stimuli and interactions, intense efforts have been devoted to designing high-performance flexible pressure sensors, in particular for typical capacitive ones that feature low power consumption to support long-term continuous detection/monitoring. However, capacitive pressure sensors essentially suffer from limitations in terms of sensitivity, linearity, and working range. Here, we report a design strategy based on contact-dominated localized electric-displacement-field-enhanced capacitance and contact mechanics to dramatically improve the sensing response and linearity of capacitive sensors over a broad pressure range. We present a novel construction of integrated sensors by employing our contact-dominated design with floating-gate low-dimensional semiconductor transistors that enables the sensor to fully exploit the transistor's on/off ratio range with enhanced sensing performance at a low operating voltage. Moreover, our sensor-equipped robotic arm demonstrates the potential to evaluate physical properties of fluids, and precisely and dynamically control to handle manipulation tasks. The proposed strategy can provide general design guidance for high-performance capacitive sensor, which would have a significant impact on human orientated future intelligent technologies.

Invited Speakers-Session 3

Xuefei Li

Huazhong University of Science and Technology, China

Biography

Dr. Xuefei Li received his PhD from Nanjing University in 2013. He was a visiting scholar at Purdue University from November 2011 to May 2013. He is currently an associate professor at Huazhong University of Science and Technology. His research focuses on advanced logic devices based on two-dimensional semiconductors. He has published over 40 papers in prestigious international journals such as Nature Electronics, Science Advances, Advanced Materials, Nano Letters, ACS Nano, and IEEE Electron Devices Letters. He demonstrated the first negative differential resistance (NDR) effect in a MoS_2 transistor due to self-heating and developed the world's first ballistic black phosphorus field-effect transistor.

Speech Title

Ballistic transport in p-type WSe_2 transistors

Abstract

To realize 2D CMOS logic circuits, p-type 2D transistors with comparable performance to that of nFETs are essential. WSe_2 is a promising 2D p-type semiconductor due to its high intrinsic hole mobility and relatively large band gap. However, the selenium vacancy in the WSe_2 film grown by CVD and the damage caused by metal contact formation can lead to undesired large Schottky barrier heights and contact resistance Rc, which severely limits the electrical performance of WSe_2 pFETs, especially short-channel devices.

In this work, we report an oxygen p-doping and full contact structure to reduce the contact resistance of monolayer p-type tungsten diselenide and demonstrate high-performance p-type WSe_2 field-effect transistors. The controllable oxygen doping and the full contact structure greatly increase the contact quality. Consequently, short-channel WSe_2 pFETs deliver a record saturation current and a ballistic ratio of 81% at room temperature. Our work presents a straightforward and versatile technique to achieve high-performance p-type two-dimensional electronics beyond silicon.

Invited Speakers-Session 3

Donglin Lu

Hunan university, China

Biography

Donglin Lu is an associate professor, doctoral supervisor, and Yuelu Scholar at the School of Physics and Electronics, Hunan University. He joined Hunan University as a postdoctoral researcher in 2020 and transitioned to the associate professor position in 2024. He has led projects including the Young Scientists Program C of the National Natural Science Foundation of China and a sub-project of the National Key R&D Program for Young Scientists. He has been recognized under talent programs such as the Furong Program for Scientific and Technological Innovation Young Talents in Hunan Province and the National Postdoctoral Program for Innovative Talents. His research focuses on novel semiconductor three-dimensional hetero-integration and interface regulation. He has published over 40 high-impact papers in journals such as Nature, Nature Communications, and ACS Nano, including a paper as first author in Nature.

Speech Title

High-density 3D integration based on 2D semiconductors

Abstract

As integrated circuit technology enters the sub-10 nm node, the practical channel length of silicon-based transistors becomes difficult to scale further, and density enhancement faces bottlenecks. Consequently, transistor integration technology is shifting from planar integration to 3D vertical integration. This report focuses on high-density 3D integration of 2D semiconductors. We propose an integrated vdW monolithic 3D integration process, in which pre-fabricated integrated vdW circuit layers and 2D semiconductor layers are stacked layer-by-layer. This approach overcomes the thermal budget limitations of monolithic 3D integration and avoids the damage to 2D semiconductors caused by traditional high-energy integration processes, achieving monolithic 3D integration of 10 circuit layers and multifunctional cooperative operation. Furthermore, we develop an exponential bisecting 3D stacking process. Planar devices on a sacrificial silicon substrate are cut in half along the midline; then one half of the device layer is separated from the substrate and bonded to the other half, forming a two-layer stacked structure. By repeating this bisecting-stacking process N times, a high-order 3D integrated system with 2^N layers is ultimately realized. Using this process, we demonstrate for the first time a 1024-layer high-density 3D chip integration, achieving an integration density of 1.5×10^9 Tr/mm^2, representing the highest number of integrated layers and the highest integration density to date.

Invited Speakers-Session 4

Yang Chai

The Hong Kong Polytechnic University, China

Biography

Prof. Yang Chai is the Chair Professor of Semiconductor Physics of the Hong Kong Polytechnic University. He is an IEEE Distinguished Lecturer, an IEEE Fellow, an Optica Fellow, IOP Fellow, and AAIA Fellow. He is the Director of Research Institute for Artificial Intelligence of Things, the Director of Joint Research Center of Microelectronics, and the Associate Dean of Faculty of Science (Research) at the Hong Kong Polytechnic University. He is also the Chair of Semiconductor Nanotechnology Alliance, the Vice President of the Physical Society of Hong Kong, and an Associate Editor of ACS Nano. He is a receipt of the Falling Walls Science Breakthroughs in Engineering and Technology for his work on "Breaking the Wall of Efficient Sensory AI Systems", the BOCHK Science and Technology Innovation Prize in the field of AI and Robotics, The Croucher Senior Fellowship, The Ho Leung Ho Lee Foundation Science and Technology Innovation Award, and NSFC Distinguished Scholar. His current research interest mainly focuses on emerging electronic devices.

Speech Title

Bioinspired In-Sensor Computing for Artificial Vision

Abstract

The demand for accurate perception of the physical world leads to a dramatic increase in sensory nodes. However, the transmission of massive and unstructured sensory data from sensors to computing units poses great challenges in terms of power-efficiency, transmission bandwidth, data storage, time latency, and security. To efficiently process massive sensory data, it is crucial to achieve data compression and structuring at the sensory terminals. In-sensor computing integrates perception, memory, and processing functions within sensors, enabling sensory terminals to perform data compression and data structuring. We will overview optoelectronic intelligence for bioinspired in-sensor computing in artificial vision. We will examine optoelectronic devices that can compress and structure multidimensional vision information, and demonstrate a few vision sensors for different scenarios, including visual adaptation, motion perception, as well as event-driven vision sensors for spiking neural network.

Invited Speakers-Session 4

Mengnan Ke

Yokohama National Univerisy, Japan

Biography

Dr. Mengnan Ke is an Associate Professor at the Institute for Multidisciplinary Sciences, Yokohama National University, Japan. He received his B.E. degree in Microelectronics from South China University of Technology in 2012 and his M.E. and Ph.D. degrees in Electrical Engineering from the University of Tokyo in 2015 and 2018, respectively. He previously worked as an Assistant Professor at Tokyo University of Science, Japan, from 2018 to 2021 and Chiba University, Japan, from 2021 to 2024. His research interests include new channel material MOSFETs, interface physics, and advanced transistor technologies. He has led multiple JST and JSPS research projects and has published several papers as the first author in IEDM and IEEE Transactions on Electron Devices.

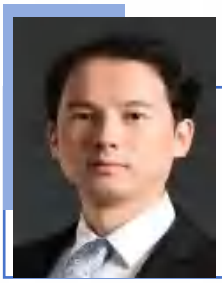
Speech Title

Understanding Slow Trap Characteristics and Degradation in GeOx/Ge MOS Structures

Abstract

Ge, with higher electron and hole mobility than Si, has attracted increasing attention as a channel material for next-generation MOSFETs. However, a large number of slow traps at GeOx/Ge MOS interfaces leads to significant reliability degradation.To understand the physical origin of slow traps in Ge MOS interfaces, we systematically investigate electron and hole traps in GeOx, Al2O3, and other high-k dielectrics, including Y2O3, HfO2, and La2O3.We demonstrate that the high density of slow traps in Al2O3/GeOx/Ge MOS structures formed by plasma oxidation can be effectively suppressed by a newly developed ALD-based Y-doping technique.

Invited Speakers-Session 5



Chuan Liu

Sun Yat-sen University, China

Biography

Chuan Liu received Ph.D. degree from University of Cambridge (U.K.) where he studied organic electronics. Then he moved to work in National Institute for Materials Science (NIMS, Japan) and then to Dongguk University (Seoul, South Korea). He is a professor and vice Dean of School of Electroincs and Information Technology, Sun Yat-sen University (China). He is mainly interested in theoretical and experimental studies in oxide and organic thin film transistors and opto-electric integration. He has published papers in Nature Electronics, Nature Communications, Science Advances, Advanced Materials and etc. He has served in the editorial board of the journal Semiconductor Science and Technology and as an associate editor of Journal of the Society for Information Display and Journal of Information Displays.

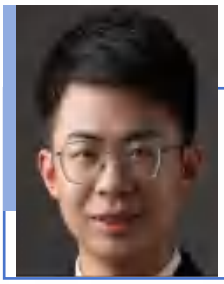
Speech Title

Advances in Metal-Oxide Thin-Film Transistors

Abstract

The advantages of organic semiconductors and oxide semiconductors are evident, as they enable the fabrication of thin-film devices at relatively low temperatures or even via solution-based methods, along with excellent bendability. However, both share a common drawback: the disorder in their crystalline structures leads to the emergence of numerous defect states. This results in significant differences in the charge injection and transport mechanisms of thin-film transistors compared to covalent silicon-based semiconductor devices. This report will preliminarily discuss the impact and analysis of defect states on thin-film transistors from the perspectives of devices and integration, as well as explore strategies to control defect states, enhance device performance, and expand circuit applications from the material and fabrication standpoint.

Invited Speakers-Session 5



Yancong Qiao

Sun Yat-sen University, China

Biography

Yancong Qiao is an associate professor in the School of Biomedical Engineering at Sun Yat-sen University. He received his B.S. degree from the Department of Electronic Science and Technology of Xi'an Jiaotong University in 2016 and his Ph.D. degree from the School of Integrated Circuits of Tsinghua University in 2021. His current research interests focus on flexible MEMS systems, biomedical micro/nano sensing, flexible electronic skins, and systems, soft robot, as well as, soft robots, etc. He has published more than 60 papers, including 27 as the first author and corresponding author in well-known journals such as Science Advances, Advanced Functional Materials, Nano-Micro Letter, InfoMat, ACS Nano, and has been cited more than 3500 times in Google Scholar. His h-factor is 30 and i10 factor is 40. He has been authorized the first inventor to hold 5 invention patents and lead multiple projects from the NSFC, Guangdong Province, and Shenzhen City.

Speech Title

Flexible Ultra-Thin Physiological Signal Sensor and Thermal-Electric Conversion System

Abstract

In recent years, flexible electronic technology has developed rapidly in the field of physiological signal monitoring. However, one important factor currently limiting the widespread application of flexible physiological signal sensors is the interface problem between the sensors and the human body. To optimize the sensor/skin interface, an effective method is realizing ultra-thin electronic skin sensor, which, on one hand, can suppress motion artifacts and improve signal quality; On the other hand, can improve the user's wearing experience, expand the amount of physiological signal database, and provide a data foundation for further integration with artificial intelligence algorithms to achieve intelligent sensors. In this report, graphene and Nanomesh is used as the core sensing materials. Laser scribing graphene is investigated to achieve device pattern and high-quality transfer technology, and multiple methods of preparing Nanomesh have been developed, based on which a series of devices such as high-sensitivity strain sensors, ultra-thin and insensitive physiological electrodes, and artificial intelligence assisted sweat sensors have been realized. Nanomesh sensors can achieve a good interface with the skin without external fixation, greatly improving the user's wearing experience. This report will also introduce flexible sensor enhancement technologies such as Nanomesh reinforcement and microcavity assistance, which greatly improve the stability, linearity, and work range of flexible mechanical sensors. Based on graphene and Nanomesh sensors, various physiological signals are collected and many databases are built. By combining with artificial intelligence algorithms, intelligent analysis and diagnosis of various physiological signals such as blood pressure, sweat output, respiration, tactile, and movement are ultimately achieved. Meanwhile, this report will also discuss the application of ultra-thin electronic skin sensors in soft robots and human-computer interaction field.

Invited Speakers-Session 6

Yutao Li

Beijing Institute of Technology, China

Biography

Yutao Li is an Associate Professor at the School of Integrated Circuits and Electronics, Beijing Institute of Technology. He received his Ph.D. from Tsinghua University in 2020. Focusing on interdisciplinary innovation, he targets key challenges of intelligent sensors in the post-Moore era using carbon-based nanomaterials, pursuing novel mechanisms, structures, and methods to enhance sensor performance and integration. He has published over 30 papers as first/corresponding author in journals such as Advanced Materials, ACS Nano, and ACS Central Science. He has served as PI for the NSFC Youth Program, Beijing Young Talent Support Project, and open research projects at national research centers.

Speech Title

Carbon-based Biomimetics Nanoelectronic Devices and Algorithmic Synergy

Abstract

Biomimetic electronics is an interdisciplinary frontier field combining biomimetic sciences and integrated microsystems. Brain-inspired neuromorphic computing and biomimetic sensors have become research hotspots. This paper focuses on two biomimetic strategies: structural biomimicry and functional biomimicry. Structural biomimicry enables dynamic visual perception and flexible tactile sensing with high sensitivity, while functional biomimicry achieves electrically and optically reconfigurable synaptic plasticity for efficient neuromorphic computing. The fabrication, working mechanism, performance characterization, and algorithmic synergy scheme of each device are elaborated respectively. Finally, this article provides prospects for the future of advanced carbon-based biomimetic nanoelectronic devices.

Invited Speakers-Session 6

Li Gao

South China University of Technology, China

Biography

Li Gao received the Ph.D degree in electrical and computer engineering from University of California San Diego (UCSD), La Jolla, California, USA, in 2020. He was a RFIC design engineer in Mediatek USA and Apple Inc. California, USA. Now he is a full professor in South China University of Technology.

He is a recipient of the Xiaomi Young Scholar award. His research interests include RF/mm-wave circuits, systems and phased-arrays. He has published more than 40 journal papers with a google scholar citations more than 2500 times with H-index of 29.

Speech Title

Millimeter-Wave Wideband/Reconfigurable Power Amplifiers and Low Noise Amplifiers

Abstract

Millimeter-wave (mmWave) technology serves as a key enabler for 5G-Advanced, 6G communications and high-precision sensing, benefiting from its ultra-wide bandwidth and rich spectrum resources. MmWave power amplifiers (PAs) and low-noise amplifiers (LNAs) are critical front-end components that determine transceiver performance in terms of output power, noise figure and bandwidth. Wideband and reconfigurable amplifier designs are increasingly required for multi-standard, dynamic mmWave systems, yet they face challenges including high-frequency parasitics, gain-bandwidth tradeoffs and process variations. This invited talk presents advanced design techniques for wideband and reconfigurable mmWave PAs and LNAs. It analyzes core design strategies, validates proposed schemes with measured results, offering practical guidance for next-generation mmWave transceiver chip design.

Invited Speakers-Session 7

Ming Qiao

University of Electronic Science and Technology of China, China

Biography

Ming Qiao, Ph.D., Professor and Doctoral Supervisor at University of Electronic Science and Technology of China (UESTC). His research focuses on power semiconductor devices, high-voltage power integration technologies, power device reliability, radiation-hardened power devices, and power device modeling. He has received two second prize of National Science and Technology Progress Awards, five provincial and ministerial-level science and technology awards, Huawei Spark Award and so on. He has authored over 200 papers and holds 16 U.S. patents and more than 100 Chinese invention patents as the first inventor. He serves on the technical program committee of ISPSD, and on the editorial board of Microelectronics Journal.

Speech Title

Customized Design of Low-Voltage LDMOS to Reduce Energy Losses for xPU Power Supply

Abstract

DrMOS based on LDMOS is a key enabler for on-chip xPU power supply. To achieve high efficiency, low-side LDMOS requires low specific on-resistance (RSP) while high-side LDMOS demands low gate-charge (QG). This talk presents a suite of customized LDMOS techniques on a 55 nm BCD platform. These include CFP and short-channel process for reduced channel resistance, grid-gate layout for higher linear current, biased split gate structures for superior RSP·QGD trade-off, and timing-controlled auxiliary gate for lower switching losses. Experimental results confirm these designs are highly suitable for next-generation DrMOS application.

Invited Speakers-Session 7

Zhihong Liu

Xidian University, China

Biography

Zhihong Liu is a full Professor at the School of Microelectronics and the Guangzhou Institute of Technology, Xidian Unviersity. He is a Senior Member of IEEE. He received his B.S. and M.S. degrees from Nankai University and the Institute of Semiconductors, Chinese Academy of Sciences, respectively, and his Ph.D. from Nanyang Technological University (NTU), Singapore. In 2007, he joined Temasek Lab (TL) at NTU as a Research Associate, where he worked on the R&D of GaN microwave devices and MMIC fabrication technologies. In 2011, he joined the Singapore-MIT Alliance for Research and Technology (SMART) as Postdoc Associate, later severing as Research Scientist and Principal Research Scientist, focusing on GaN microwave/mm-wave/THz devices, GaN–Si CMOS heterogeneous integration technologies, and GaN power electronic devices. He joined Xidian University, China as a full Professor in 2019. From 2020-2025, he served as the founder and Executive Director of the Guangzhou Wide-Bandgap Semiconductor Innovation Center (GWSIC) at Xidian University. His current research interests include wide-bandgap and ultra-wide-bandgap semiconductor electronic devices and integrated circuits, with a particular focus on advanced GaN-based technologies.

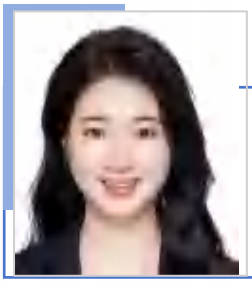
Speech Title

Progress of GaN-on-Si RF Devices

Abstract

As a wide-bandgap semiconductor, GaN offers broad application prospects in RF fields such as radar, satellite, and 5G/6G communications. Benefiting from the advantages of GaN-based semiconductors, including a high critical electric field, high 2DEG concentration, high electron mobility, and high saturation velocity, GaN electronic devices and integrated circuits (ICs) possess excellent characteristics such as high output power, high efficiency, high-temperature operation ability etc. GaN grown a Si substrate, so called GaN-on-Si, combines the performance of GaN and the advantages of Si substrates, offering low cost, large-wafer availability, and the potential for mass production. In this talk, we will provide an overview of our recent research progress in GaN-on-Si RF devices and MMICs. Key topics include fabrication technology for 6-inch wafer C-to-Ka band GaN-on-Si device and MMICs, GaN mm-wave and THz power and low-noise transistors, and low-voltage GaN-on-Si RF devices for mobile terminal applications.

Invited Speakers-Session 8



Yuanyuan Shi

University of Science and Technology of China, China

Biography

Dr. Yuanyuan Shi currently works at University of Science and Technology of China (USTC) as a professor in the school of Integrated Circuits. Before joining in USTC, she was a senior researcher at IMEC, Belgium. She received her Ph.D. degree (with Excellent "Cum Laude" Honor and Extraordinary PhD prize) from University of Barcelona in 2018. Her research interests focus on 2D and oxide semiconductors based thin-film transistors for logic, memory and brain-inspired computing. Dr. Shi has published more than 70 research articles (including Nature Electronics, IEDM, VLSI, ACS Nano, etc.), two book chapters and five international patents, etc. She served as a committee member for IEEE EDS Nanotechnology committee and several IEEE flagship conferences, including IRPS, EDTM and IPFA. Dr. Shi also serves as an active reviewer for Nature, Nature Electronics, Nature Materials, Nature Communication, ACS Nano, IEEE Electron Device Letters, and others. Dr. Shi is a recipient of Marie Skłodowska-Curie Individual Fellowship (European Commission), IEEE EDS PhD student fellowship (three winners globally each year), ADF-The Rising Stars Women in Engineering, Forbes 30 under 30 (Forbes), Park AFM award (Park Systems), etc.

Speech Title

2D-semiconductor transistors for advanced logic and memory devices: from channel deposition to device integration

Abstract

Abundant-data computing such as big-data analytics, artificial intelligence (AI) and Internet of Things (IoT) demand extreme energy efficiency and concomitant improvement of cost performance of the electronic systems. Field-effect transistors (FETs) represent the fundamental building blocks for modern computer processors. The number of transistors in a typical microprocessor has followed a remarkable exponential growth since the 1960s, a trend known as Moore's law. By making the device smaller, more transistors can be packed into a single chip with much improved performance and reduced cost. The continued miniaturization of silicon microelectronics has fuelled the exponential growth of the integrated circuits for over half a century. Today, as silicon transistors enter the sub-10nm technology node with increasing technical challenges, the exploration of alternative device geometries or new channel materials is ever more important for future processor chip. Atomically thin two-dimensional (2D) semiconductors have attracted tremendous interest as a new channel material that could facilitate continued transistor scaling. To benefit from continuous scaling, the performance of the scaled 2D transistors needs to outperform Si technology nowadays. However, significant efforts are still required for channel material deposition, gate stack development and CMOS integration, etc. This talk will present our recent progress on 2D semiconductors based logic and memory devices, including selective-area deposition of high-quality channel, scaled-device integration and 2T0C DRAM application etc.

Invited Speakers-Session 8

Bobo Tian

East China Normal University, China

Biography

Bobo Tian is a professor at the Key Lab of Polar Materials and Devices (MOE), East China Normal University since 2019. He was selected by Excellent Young Scientists Fund awarded by the National Natural Science Foundation of China (NSFC) in 2022. He is now the director assistant of Shanghai Center of Brain-inspired Intelligent Materials and Devices, Shanghai, China. His group is currently working on ferroelectric memory and neuromorphic computing. He has published over 140 papers in journals such as Nat. Mater., Nat. Sens., Nat. Electron., and Nat. Commun. etc.

Speech Title

Ferroelectric devices for in-memory computing

Abstract

Inspired by neurobiological systems, in-memory and in-sensor computing technologies provide a new means of overcoming the limitations inherent in the von Neumann architecture. The basis of neural morphological computation is a crossbar array of high-density, high-efficiency nonvolatile memory devices. Of the numerous candidate memory devices, ferroelectric memory devices with nonvolatile polarization states, low power consumption, and strong endurance are expected to be ideal candidates for neuromorphic computing. Here I give a talk based on our recent reports about ferroelectric in-memory computing devices.

Invited Speakers-Session 9

Jiewei Chen

South China Normal University, China

Biography

Jiewei Chen is a Professor at the School of Optoelectronic Science and Engineering, South China Normal University. He has long been engaged in research on novel information materials, new-concept optoelectronic devices, and bio-inspired optoelectronic chips, with a focus on sensing-computing fusion chips for low-power smart IoT and flexible photonic chips. He has led several major projects, including the National Key R&D Program Young Scientists Project and the General Program of the National Natural Science Foundation of China. As a corresponding or first author, he has published a series of papers in top-tier journals such as Nature Nanotechnology, Science Advances, Nature Communications, and Advanced Materials. His research on bio-inspired visual chips was recognized among the "Chip Top Ten Advances in Chinese Chip Science" and has received positive highlights in Nature and Nature Materials.

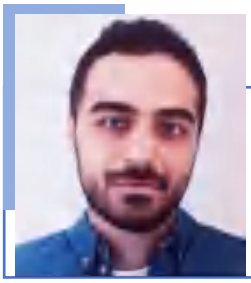
Speech Title

Bioinspired Neuromorphic Devices for Broadband Dynamic Information Encoding and Recognition

Abstract

Beyond conventional pixel-dense imaging systems, bioinspired neuromorphic optoelectronic devices offer a pathway toward low-power, high-efficiency broadband dynamic perception. By leveraging asymmetric two-dimensional molecular-crystal heterojunctions, we overcome the intrinsic linear dichroic ratio limit of single-layer architectures, achieving a record-high polarization sensitivity (LDR up to 10.3) for self-powered graded analog sensing and temporal encoding. Complementarily, monolithically integrated wafer-scale telluride semimetal/germanium photodetectors enable room-temperature mid-infrared detection up to 10.6 μm with high detectivity (>10^{10} cm·$Hz^{1/2}$·W^{-1}) and micrometer-scale trajectory tracking resolution. In-sensor computing strategies—including nonlinear summation, temporal integration, and 400× data compression—allow sparse sensor arrays to perform real-time multiclass dynamic target recognition with over 95% accuracy under challenging scenarios such as rain, fog, and low contrast. This work establishes a general platform for wide-spectrum, low-power, and intelligent motion perception, directly advancing next-generation autonomous vision and smart IoT systems.

Invited Speakers-Session 10



Mohammad Samizadeh Nikoo

Nanyang Technological University, Singapore

Biography

Mohammad Samizadeh Nikoo is a Nanyang Assistant Professor in the School of Electrical and Electronic Engineering (EEE) at Nanyang Technological University (NTU), Singapore. He is the founding director of the Innovative Electronic & Electromagnetic Device Laboratory (i–Lab). He received his PhD from EPFL, Switzerland, in 2022. In the same year, he joined the Integrated Systems Laboratory at ETH Zurich as a research scientist, before beginning his tenure-track appointment at NTU in 2023. Dr. Samizadeh Nikoo is a Fellow of the National Research Foundation, Singapore (Class of 2024). He has received several distinctions and awards and currently serves as the lead principal investigator (PI) on multiple national research projects. His research focuses on developing a new generation of high-frequency semiconductor components for future information technologies.

Speech Title

High-Performance Electronic Metadevices for Millimeter-Wave and Terahertz Integrated Circuits

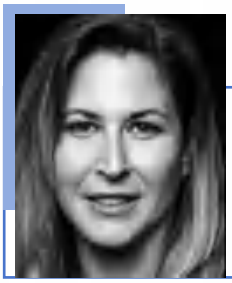
Abstract

Approaching the terahertz band from the electronics side is of great technological importance, with the promise of advancing next-generation wireless communication systems toward 6G and beyond. However, inherent limitations of high-speed transistors, the primary building blocks of monolithically integrated high-frequency circuits, have hindered the realization of high-performance terahertz electronics.

Electrical metastructures offer an alternative paradigm, in which modulation of the conductivity of a semiconducting layer controls collective quasi-electrostatic responses within a lumped structure, enabling electronic functionalities such as switching, mixing, and parametric amplification. Compared with conventional transistors, electrical metastructures enable ultra-low contact resistances, leading to record-high switching cutoff frequencies well beyond 10 THz in a compact device platform, referred to as electronic metadevices.

The first part of this talk highlights recent advances in III-nitride electronic metadevices operating up to 1 THz and introduces a new generation based on quasi-one-dimensional electrical metastructures with enhanced electrical performance. We present theoretical insights into the collective responses governing the operation of electronic metadevices and elucidate their ultimate performance limits. In the second part, we introduce a metastructure-based paradigm for directly realizing high-performance millimeter-wave and terahertz components with ultracompact footprints, demonstrated the compatibility of metatronic devices with commercial silicon processes.

Invited Speakers-Session 11



Eleni Makarona

Institute of Nanoscience and Nanotechnology, NCSR “Demokritos”, Greece

Biography

Dr. Eleni Makarona is Director of Research at the Institute of Nanoscience and Nanotechnology, NCSR "Demokritos", Greece. She holds a PhD in Physics from Brown University (USA), where she trained under Prof. Arto V. Nurmikko on III-nitride optoelectronics, supported by a competitive graduate fellowship awarded to the top 10% of international applicants.Her research spans two parallel axes maintained continuously for nearly two decades: silicon photonic biosensors, and chemically synthesized metal oxide nanostructures. Her work on photonic sensors spans applications in biodiagnostics, food safety and quality assurance, and environmental monitoring. Moreover, she is co-inventor of the Broadband Mach-Zehnder Interferometer and Broadband Young Interferometer detection architectures — novel sensing principles that progressed from fundamental invention through patents to international prototype deployment. In metal oxide nanostructures, her work follows a material-first philosophy in which device concepts emerge from deep understanding of defect-driven mechanisms, spanning optoelectronics, sensing, energy harvesting, and hardware security. She has led or coordinated competitive research programs across European and national frameworks, and has delivered invited presentations at international conferences. She was awarded the Greek L'Oréal–UNESCO Award For Young Women in Science in 2010.

Speech Title

Scalable Functional Devices Based on Chemically Synthesized ZnO Nanostructures: Bridging Synthesis and Device Functionality

Abstract

Low-cost, chemically synthesized metal oxide nanostructures offer a compelling pathway toward scalable, cost-efficient, and sustainable electronic and sensing devices. However, building functional devices from such nanostructures requires more than mastering fabrication and compatibility with standard micro/nanofabrication processes — it demands a deeper understanding of the underlying physical mechanisms governing the material itself and of how these translate into, and ultimately dictate, device performance.This talk presents a device-oriented framework in which zinc oxide (ZnO) serves as a representative material platform. Central to this framework is the systematic investigation of defect-driven mechanisms emerging from the growth environment — mechanisms that, contrary to conventional device design assumptions, are shown to be the dominant determinants of functional behavior rather than structural geometry or intentional doping alone.This perspective enables the development of functional systems across diverse application domains. Representative implementations span ZnO-based homojunction devices, sensing platforms exploiting defect-mediated mechanisms, energy harvesting systems, and hardware security elements. Collectively, these demonstrate a coherent, fabrication-compatible, and scalable pathway for functional device realization from chemically synthesized nanostructures — one that redefines material imperfection not as a limitation to be suppressed, but as a design parameter to be understood, controlled, and exploited.

Invited Speakers-Session 11

Daquan Zhang

The Chinese University of Hong Kong, Shenzhen, China

Biography

Dr. Daquan Zhang is an Assistant Professor in the School of Science and Engineering at The Chinese University of Hong Kong, Shenzhen. He earned his B.Eng. degree and Ph.D. degree from Wuhan University in 2014 and HKUST in 2020, respectively. After that, he worked as a Research Associate and Research Assistant Professor at HKUST from 2020 to 2024. His research focus is on the growth and carrier dynamics study of metal halide perovskite nanomaterials and their applications in high-performance optoelectronic devices. He has published over 50 journal articles, with first-/corresponding-author papers in *Nature Photonics, Advanced Materials, Nano Letters, NPJ Flexible Electronics, etc.*

Speech Title

Metal halide perovskite nanowire arrays for high-performance optoelectronic devices

Abstract

Metal halide perovskite (MHP) nanowires (NWs) have energized remarkable research interests owing to their unique characteristics of grain-boundary-free, efficient axial carrier transportation, and strong radial spatial-confinement. However, low photoluminescence quantum yield (PLQY) is usually achieved in MHP NWs because of severe surface non-radiative recombination, which limits their applications in high-performance optoelectronics, such as photodetectors (PDs), solar cells, lasers and light-emitting diodes (LEDs). Here, vertically aligned, high-quality and ultrahigh-density MHP NW arrays have been fabricated in porous alumina membranes with vapor-phase and solution-phase strategies. The obtained MHP NWs possess significantly high (>90%) PLQY and excellent chemical stability. The fabrication is also compatible with large-scale rigid and flexible substrates. Consequently, they have been fabricated into high-performance and flexible optoelectronic devices, including LEDs, narrowband and self-powered PDs, etc. These results suggest that the MHP NWs are highly promising to broaden the development of MHP nanomaterials and promote their practical applications in high-performance optoelectronics.

Invited Speakers-Session 12

Sunbin Deng

Huazhong University of Science and Technology, China

Biography

Dr. Sunbin Deng received his B.Sc. degree from Huazhong University of Science and Technology (HUST), Wuhan, China, in 2014, and his Ph.D. degree in Electronic and Computer Engineering from the Hong Kong University of Science and Technology (HKUST), Hong Kong SAR, in 2020. Subsequently, he held postdoctoral fellow positions at Purdue University (2021–2022) and Georgia Institute of Technology (2022–2025). Dr. Deng is currently a Professor at the School of Optical and Electronic Information, HUST. His research focuses on back-end-of-line (BEOL)-compatible thin-film (opto-)electronics, with a particular emphasis on oxide semiconductor transistors, for monolithic 3D integration, electronic-photonic integration, alternative computing, and information display technologies. To date, Dr. Deng has co-authored 80+ publications, including 30+ papers as first or corresponding author, in leading peer-reviewed journals (e.g., Sci. Adv., Nat. Commun.) and top-tier international conferences (e.g., IEDM, VLSI). He has received several academic awards, including the Distinguished Paper Award at SID Display Week Symposium and the Young Leader Award from SID.

Speech Title

BEOL-Compatible Oxide Power Transistors for On-Chip Active Power Delivery Networks in 3D ICs

Abstract

Increasing power demands and the presence of multiple supply voltage domains pose unprecedented challenges for power delivery in 3D integrated circuits (ICs). Distributing integrated voltage regulators (IVRs) throughout 3D ICs to realize active power delivery networks (PDNs) offers a scalable and energy-efficient solution. In this talk, I will introduce back-end-of-line (BEOL)-compatible amorphous oxide semiconductor (AOS) power transistors as a competitive active device technology for on-chip voltage conversion. Significant recent advances in AOS materials, device structures, and fabrication processes have substantially improved transistor performance and reliability. As a result, ITO planar power transistors with a specific on-resistance (Ron,sp) as low as 87 mΩ·mm² have enabled the experimental demonstration of switched-capacitor DC-DC converters, which achieved a stage efficiency of ≥87.5% for 2:1 step-down conversion from 12 V. Furthermore, by developing IGO vertical power transistors with an ultralow Ron,sp of 0.04 mΩ·mm², the converters operating at a 3 V voltage rating could achieve a simulated peak stage efficiency of 94.3%. These results highlight the great potential of AOS power transistors for enabling highly efficient IVRs and, ultimately, active PDNs in 3D ICs.

Invited Speakers-Session 12

Dexing Liu

The Chinese University of Hong Kong, Shenzhen, China

Biography

Dr. Dexing Liu obtained his B.S. in Applied Physics from Shandong University in 2020 and earned his Ph.D. in Integrated Circuit Science and Engineering from Peking University in 2025. In 2024, he was a visiting scholar in the Department of Applied Physics at The Hong Kong Polytechnic University. He is currently a postdoctoral fellow at The Chinese University of Hong Kong, Shenzhen. His research focuses on semiconductor device physics, post-Moore era electronic devices, and design-technology co-optimization. To date, he has published nearly ten (co-)first-author papers in journals such as Nature Nanotechnology and Advanced Materials, with over 20 SCI publications and more than 400 citations. He has received multiple awards, including the National Scholarship, Beijing Outstanding Graduate, Peking University Outstanding Graduate, Baidu ERNIE Science and Technology Innovation Star Award, and Shenzhen Outstanding Academic Paper Award.

Speech Title

Making Efficient Electrical Contacts in Low-Dimensional Semiconductors

Abstract

The performance of low-dimensional semiconductors, which are pivotal for post-Moore nanoelectronics, is severely limited by high contact resistance and poor metal-semiconductor interfaces. To overcome these bottlenecks, we introduce Mc4 (Making Clean, Close, Complementary Contacts), a systematic framework for atomic-level interface engineering. The multidisciplinary approach combines theoretical modeling, interface modulation, and experimental validation to achieve two key advances. First, the discovery of a quantum limit in contact resistance enabled by hydrogen-bonded, non-covalent contacts that mitigate Fermi-level pinning and contamination. Second, a flexible integration strategy producing MXene-based hydrogen-bonded heterojunctions with outstanding charge transport and durability, as evidenced by CNT transistors retaining 74 cm2 V-1 s-1 mobility after 100,000 bending cycles. This work bridges atomic precision with scalable fabrication, offering a universal pathway toward high-performance low-dimensional flexible electronics.

Invited Speakers-Session 14

Chunlei Wu

Fudan University, China

Biography

Prof. Chunlei Wu is an Associate Professor with the School of Microelectronics, Fudan University. Her research interests include in the area of post-Moore emerging logic devices, focusing on advanced Gate-All-Around FET, Complementary FET, etc. She has authored/co-authored more than 60 technical papers in international journals and conferences, held 16 granted patents.

Speech Title

Physical Modeling of the Subthreshold Swing Saturation Behavior in Cryogenic MOSFETs

Abstract

Accurate device modeling is crucial to cryogenic CMOS technology development for future quantum computing applications. The existing band tail-based models, however, arbitrarily assume an unchanged band tail states distribution at deep cryogenic temperature, resulting in significant modeling error of the subthreshold swing (SS) saturation behavior in cryogenic MOSFET. In this work, a novel band tail model featuring a temperature-dependent band tail states distribution has been presented and verified. The introduction of temperature sensitive distribution of tail states enables accurate modeling of the SS saturation value and the critical temperature corresponding to SS deviation. The results provide a deeper insight into the physical mechanisms study and modeling of cryogenic MOSFETs.

Invited Speakers-Session 15

Qianqian Huang

Peking University, China

Biography

Prof. Qianqian Huang is a Full Professor with Tenure in the School of Integrated Circuits at Peking University. Her research interests are in the area of emerging low-power devices for diverse applications, in particular tunnel devices and ferroelectric devices. She has authored/co-authored more than 100 technical papers in international journals and conferences and held more than 70 granted patents. She is the recipient of Chang Jiang Scholar (2023), the Chinese Young Women in Science Award (2022), Xplorer Prize (2020), IEEE EDS Early Career Award (2019), etc.

Speech Title

Si Hybrid Tunnel FET-CMOS Foundry Platform for Ultra-low-Power Circuit Applications

Abstract

This work demonstrates the recent progress on 55 nm Tunnel FET(TFET)-CMOS hybrid integration platform and its ultra-low-power circuit applications. By integrating the bulk-Si-based novel dopant-segregated TFET (DS-TFET) with large ION and record high ION/IOFF ratio, as well as the novel laminated isolation technology into the CMOS baseline technology, energy-efficient TFET-CMOS hybrid circuits are experimentally realized. 1Kbit TFET-Gated-Ground SRAM is implemented and demonstrated in MCU always-on domain showing sub-100nA ultra-low leakage, and a 6T hybrid TFET-CMOS SRAM-based digital CIM accelerator is designed showing high energy efficiency without performance or area penalty. Moreover, a novel DS-TFET-like device (AsyFET) with ultralow off-state leakage current and bidirectional conductivity is further demonstrated as the write transistor of 2T0C eDRAM, leading to the long retention of 3.9 s in 55nm technology node. The TFET-CMOS hybrid platform of this work demonstrates the great potential for cutting-edge power-dieting applications.

Invited Speakers-Session 15

Qiming Shao

The Hong Kong University of Science and Technology, China

Biography

Qiming Shao received his Bachelor's degree in 2013 from Tsinghua University and his Ph.D. in 2019 from University of California, Los Angeles (UCLA).

His lab aims to realize energy and time-efficient hardware using spintronic and quantum materials for physical and quantum intelligence. Currently, his lab is focusing on novel electronic and spintronic materials and their hardware-software co-design for memory, AI, robotic, and quantum computing applications. His research works are published in top peer-reviewed journals and conferences, including Nature Electronics, Nature Materials, and International Electron Device Meeting (IEDM).

He is a recipient of 2022 IEEE Magnetics Society Early Career Award and UCLA Distinguished PhD Dissertation Award.

He is currently the chair of the IEEE Magnetics Society Hong Kong Chapter (since 2023) and the IEEE Electron Devices Society Young Professionals Committee (since 2024). He was the chair of the IEEE Hong Kong Electron Devices/Solid-State Circuits Joint Chapter (2021-2022). He has served as chair or member of sub-committees for several international conferences, such as IEDM and EDTM. He is an associate editor of npj Spintronics, Springer Nature.

Speech Title

Scaling probabilistic computing for AI and optimization

Abstract

As Moore's Law reaches its limits, CMOS+X (X stands for a CMOS-compatible nanotechnology) architecture emerges as a key direction for future computing. Probabilistic computing is crucial for solving real-world generative AI tasks and combinatorial optimization problems (COPs). The digital CMOS Ising machine is constrained by massive data movement and requirements for pseudo-random number generators (PRNGs) and look-up table (LUT) circuits. The memristor crossbar-based and sMTJ-based Ising machines accelerate deterministic and probabilistic computing, respectively. However, conventional mix-signal CMOS+X schemes introduce additional overheads, such as DACs or ADCs, and the requirement of P-bits sampling. Here, we present our generative AI hardware and fully analog in-memory annealing Ising machine based on CMOS-integrated voltage-controlled magnetic anisotropy magnetic tunnel junction (VCMA-MTJ), developed through a device-circuit-system co-design approach to address bottlenecks in traditional digital CMOS and mixed-signal CMOS+X Ising machines. We leverage the VCMA effect to control the energy barrier of the VCMA-MTJ, enabling it to function as either a C-bit (stable storage for the coupling weight) or a P-bit. For the general AI hardware, we use in-memory computing to perform the multiply-accumulate (MAC) operation and random dropconnect method to emulate stochastic neural equations in situ with external P-bit sampling and transfer. For analog Ising machine, we directly implement the matrix-vector multiplication between the spin and coupling vector within the array, eliminating the need for P-bit sampling. We fabricated a VCMA-MTJ array chip integrated with 28-nm CMOS technology and developed a fully analog in-memory annealing Ising machine prototype. We validated the functionality and analyzed the performance of the proposed Ising machine using a 32-node Max-Cut problem. Acknowledgement: This research was supported by ACCESS – AI Chip Center for Emerging Smart Systems, sponsored by the InnoHK initiative of the Innovation and Technology Commission of the Hong Kong Special Administrative Region Government, TRS (T46-705/23R), VP2020S25EG15, and NSFC Cat B (62522410).

Invited Speakers-Session 16

Cher Ming Tan

Chang Gung University, China

Biography

Professor Cher Ming Tan is a leading authority in reliability engineering, currently serving as a Professor at Chang Gung University (Taiwan) and Director of the Reliability Science and Technology Center. Since 2024, he has also held the presidency of the Taiwan Reliability Technology Promotion Association. His career began in 1984 at Fairchild Semiconductor, followed by pivotal roles at Hewlett-Packard and Chartered Semiconductor, which built his cross-disciplinary expertise in materials, devices, and system-level reliability before he transitioned to academia in 1996.

Professor Tan is a Senior Member of IEEE and a Fellow of several prestigious institutions, including the Singapore Quality Institute, Institute of Engineers, Singapore and the International Association of Advanced Materials, Swedan. He is a contributor to international standards like IEEE 1624 and IEEE 1413. Since 2007, he has served as an IEEE EDS Distinguished Lecturer, delivering over 40 keynote addresses and providing systematic reliability training at major conferences such as IRPS, RAMS, and EDTM.

He has Published over 400 papers in high-impact journals and authored 14 books on reliability, with his work on Simulated Annealing exceeding 60,000 downloads. He is recognized among Stanford University's Top 2% Scientists worldwide, specifically ranking in the top 0.043% for Semiconductor Reliability. He also provided expert consulting to more than 50 international organizations, including NASA, TSMC, Microsoft, the Taiwan Space Agency, and Aptiv.

Speech Title

A Multi-Physics Toolkit for Predictive Electromigration Modeling in Advanced IC Interconnections

Abstract

As semiconductor technologies advance toward complex chiplet integration and extreme miniaturization, the reliability of integrated circuit (IC) interconnections has emerged as a primary bottleneck for system performance. High current densities in these scaled interconnects make electromigration (EM) a critical failure mechanism. However, traditional assessment methods, such as Black's Equation, are increasingly inadequate; they lack the capability to localize void-nucleation sites or effectively couple the complex 3D multi-physics driving forces—specifically thermal and thermo-mechanical stress gradients—present in realistic structures.

This talk introduces an advanced simulation toolkit developed as an Ansys Customization Toolkit designed for the rapid and accurate assessment of interconnect reliability. By utilizing a dynamic Atomic Flux Divergence (AFD) formulation derived from the first principles of thermodynamics, the toolkit captures the spatial-temporal evolution of EM-induced degradation.

A key innovation of this toolkit is its integration of microscale defect dynamics and energy barriers—parameters often experimentally inaccessible—computed via Density-Functional Theory (DFT) and Finite-Element Analysis (FEA). This enables the modeling of synergistic effects between electron-wind, thermal gradients, and stress-migration in a full 3D environment. With such ab-initio modeling, strong correlation between estimated failure times and experimental data, achieving low error rates for Copper (0.37%) and Aluminum (0.27%) interconnects are observed. This toolkit can facilitate the evaluation of novel materials, barrier metals, and layouts before committing to resource-intensive back-end-of-line (BEOL) process development.

By providing a robust predictive framework, this toolkit serves as a vital tool for optimizing reliability and accelerating the development cycle of advanced integrated systems.

Invited Speakers-Session 17

Yeliang Wang

Beijing Institute of Technology, China

Biography

Dr.Yeliang Wang is a full professor and the Dean in School of Integrated Circuits and Electronics, Beijing Institute of Technology. He received his B.S. and M.S. degree from the Wuhan University of Technology, Ph.D. degree from Institute of Physics(IoP), Chinese Academy of Sciences (CAS). He then joined in the Max-Planck-Institute for Solid Research, Germany as a Humboldt Fellow (hosted by Prof. Klaus Kern). He was appointed an associate professor in 2008 and a full professor in 2013 in the IoP, CAS. He set up a research group in Beijing Institute of Technology (BIT) in 2018. He was awarded as the National Science Fund of China for Distinguished Young Scholars. His current research interest is the controlled growth, quantum properties and funtional nanodevices of novel two-dimensional materials and heterostructures. He held more than 310 papers published on high-profile journals.

Speech Title

Tunning Properties of Novel 2D Heterostructures & Devices

Abstract

The novel properties of graphene honeycomb structure have spurred tremendous interest in investigating other two-dimensional (2D) layered structures beyond graphene for nanodevices. In this talk, I will mentioned the fabrication and properties of several 2D materials such as magnetic VSe_2 monolayer, semiconducting $PtSe_2$ monolayer, charge density wave $NbSe_2$ superstructure and related heterostructures and devices, as well as quantum properties for nanoelectronics and valleytronics will also be introduced. In addition, the stacking heterolayers for ultrahigh denisty information storage, Majorana bound states and quantum computing will be also presented. Complex micro-nano architectures with high spatial resolution and tunable depth profiles are also realized by new lithography technique.The precise structural configurations at atomic-resolution of these materials and device transport properties will also be introduced.

Invited Speakers-Session 17

Jiuren Zhou

Xidian University, China

Biography

Jiuren Zhou is a Professor and Ph.D. Supervisor at Xidian University. He has been selected for China's National Young Talent Program, recognized as a Xiaomi Young Scholar, and certified as a Category-B High-Level Talent of Hangzhou. He received his B.Eng. and Ph.D. degrees from Xidian University under the supervision of Academician Yue Hao. During his doctoral training, he conducted joint research at the University of California, Berkeley, working with Prof. Sayeef Salahuddin and Prof. Chenming Hu, and later carried out research at the Silicon Nano Device Laboratory (SNDL) of the National University of Singapore. He is currently a core member of the research team led by Academician Yue Hao and Prof. Genquan Han at the Hangzhou Institute of Xidian University.

His research focuses on emerging ferroelectric memories, in-memory computing devices, and advanced computing chips. He has published over 100 papers in leading microelectronics journals and conferences, including IEEE IEDM, VLSI, EDL, and TED. He authored the monograph Negative Capacitance Field-Effect Transistors and holds more than 30 invention patents. He has led three national-level research projects, including a sub-project of the Science and Technology Innovation 2030 Program, and has received multiple academic honors.

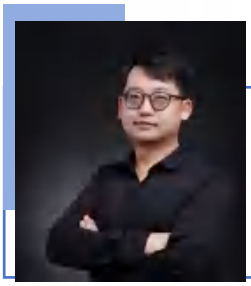
Speech Title

>10^{10}-Cycle Endurance in Wurtzite Ferroelectrics via a Superlattice and Recovery Protocol Enabling Vacancy Confinement

Abstract

Wurtzite-structured ferroelectrics offer distinct advantages for ultra-high-density, large-scale integrated memory due to their quasi-single-crystalline three-dimensional lattice architecture. However, their application is fundamentally constrained by endurance degradation under electrical cycling, with fatigue failure typically occurring before 10^8 cycles. The underlying microscopic mechanisms remain poorly understood. Here, we identify nitrogen vacancy (V_N) clustering and long-range vertical migration as primary contributors to endurance breakdown. To address this, we design a spatially engineered AlScN/AlN superlattice coupled with a dynamic recovery protocol, jointly suppressing V_N accumulation and mobility in both spatial and energetic domains. This combined approach stabilizes the defect distribution under high-field cycling, mitigating dielectric breakdown and polarization degradation. Consequently, we demonstrate ferroelectric endurance exceeding 10^{10} cycles in a wurtzite system—surpassing prior records by two orders of magnitude. This work clarifies the fatigue-inducing role of V_N and establishes a structural–defect co-engineering strategy for highly reliable ferroelectric devices.

Invited Speakers-Session 18



Kanhao Xue

Huazhong University of Science and Technology, China

Biography

Kanhao Xue is a professor at School of Integrated Circuits, Huazhong University of Science and Technology. He received his Bachelor's degree from the Department of Electronic Engineering, Tsinghua University, and his Master's degree from the Institute of Microelectronics, Tsinghua University, where he was honored as an Outstanding Master's Graduate of Tsinghua University in 2007. From 2007 to 2010, he pursued his Ph.D. at the University of Colorado Colorado Springs, under the supervision of Professor Carlos A. Paz de Araujo. He has published over 170 papers in international journals. He has been listed as an Elsevier top 2% most-cited scientist worldwide. In 2018, he proposed a density functional theory-based band structure calculation method called shell DFT-1/2, which has been adopted by Synopsys in its QuantumATK simulation software. This method primarily addresses the inaccuracy of density functional theory in calculating semiconductor band gaps and extends the DFT-1/2 approach to achieve good performance for covalent semiconductors as well. In 2023, he proposed the seven-coordination theory for the origin of hafnium-based ferroelectricity. In 2024, he proposed a brand-new classification method for inorganic ferroelectric materials. In 2025, he proposed the occ DFT-1/2 method suitable for the electronic structure calculation of two-dimensional materials.

Speech Title

On the direct bandgap of GaN and indirect bandgap of GaP

Abstract

The direct band gap feature of GaN seems at first glance not very crucial for its power electronics applications. Yet, in case its conduction band minimum falls along the Gamma-X line like Si or Ge, it will possess much lower electron mobility. The 3d electron shell of Ga has proven significant to the direct gap feature since it pushes up the zone boundary energy eigenvalues much heavier than the zone center, through p-d repulsion, for the conduction band. Nevertheless, it is still difficult to understand the fact that both GaN and GaAs show direct bandgap while GaP suffers from an indirect gap. In this talk, we show that the direct gap feature of GaN is related to strong Coulomb attraction from the N nucleus, exerting on the conduction band electron. It is the covalent bonding feature that allows for such electron to emerge, with a nonnegligible probability, in the 2p orbital of N. In contrast, the 3p orbital of P is much farther from the nucleus, which fails to convert GaP into a direct gap semiconductor. The self-energy potential, which stems from the DFT-1/2 method, has been used to hypothetically perturb the electronegativity of elements, thus revealing the mechanism in a more vivid manner.

Conference Guidelines

Conference Guidelines

Conference Venue

EDSSC 2026 will be held in The Xanadu Guanzhou Hotel, Guangzhou, Guangdong, China from Jun 9-12, 2026.

Address: No.1 Xing Dao Huan Nan Road, International Bio Island, Guangzhou City, Guangdong

Tel: +86- 020-89068888

Transportation Guide

* Guangzhou Baiyun International Airport

≈50 km, 60 minutes

* Guangzhou South Railway Station

≈26 km, 40 minutes

* Guangzhou East Railway Station

≈16 km, 30 minutes

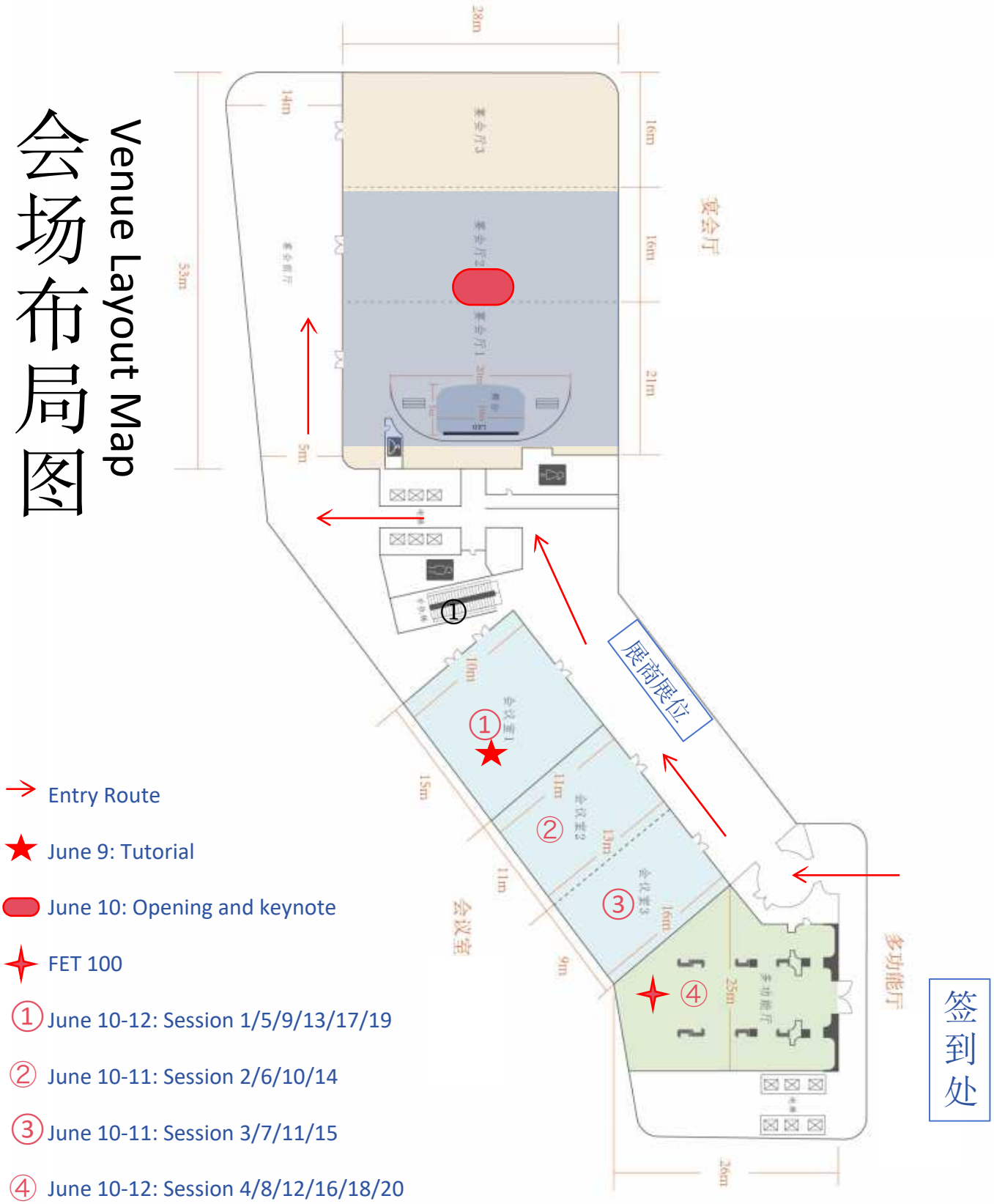
Conference Resources

QR Code for Conference Website

QR Code for Live Photo Gallery

Conference Guidelines

会场布局图 Venue Layout Map



→ Entry Route

★ June 9: Tutorial

⬭ June 10: Opening and keynote

✦ FET 100

① June 10-12: Session 1/5/9/13/17/19

② June 10-11: Session 2/6/10/14

③ June 10-11: Session 3/7/11/15

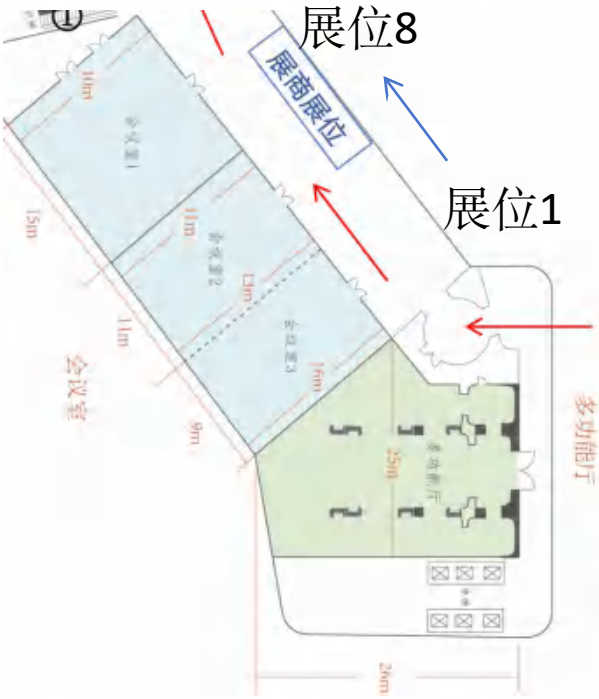
④ June 10-12: Session 4/8/12/16/18/20

Conference Guidelines

We are pleased to welcome you to the Exhibitor Area, where leading companies in precision instrumentation, intelligent testing, optical technology, and electronics are gathered. This is a great opportunity to engage directly with exhibitors, explore the latest products and technological innovations, and discuss potential collaboration. Please feel free to visit the booths and connect with our exhibitors — together, let's explore new opportunities for development in the industry.

本次会议特别设置行业展商展示区，汇聚了来自全国多家优秀的科技与仪器企业，涵盖精密仪器、智能测试、光学技术、电子科技等多个前沿领域。您可以在此与展商面对面交流，了解最新产品与技术动态，拓展合作机会。欢迎前往各展位与展商互动交流，共同探索行业发展新机遇。

会议展商展位分布图



会议展商名单

展位1	展位2	展位3	展位4	展位5	展位6	展位7	展位8
英铂科学仪器（上海）有限公司	托托科技（苏州）有限公司	广州市君威科学仪器有限公司	MDPI	中科睿华科技（北京）有限公司	北京金竞科技有限责任公司	深圳市华芯测试科技有限公司	卡尔蔡司（上海）管理有限公司

Organization

Host

Through a century of trials and triumphs, South China University of Technology (SCUT) has flourished, nurturing generations of distinguished talent. Tracing its roots back to the Guangdong Provincial First-Class Industrial School a century ago, SCUT was formally established in 1952 as one of the “Four Institutes of Technology” in China. Over the decades, SCUT has forged ahead with reform and confidently stepped forward remaining to its original mission: to build up a world-class university and nurture top-tier talents. Guided by SCUT’s motto and upholding a tradition of academic excellence, generations of SCUT graduates have grown into remarkable engineers, entrepreneurs and scientists, contributing their wisdom and strength to the rise of the Guangdong-Hong Kong-Macao Greater Bay Area, the rejuvenation of our nation, and the progress of humanity.

SCUT is located in Guangzhou with three campuses, where technology and humanities merge, tradition and modernity shine together in harmony. SCUT is a hall of academic freedom, characterized by a vibrant academic atmosphere, outstanding research, and renowned scholars. This is a dynamic stage for nurturing well-rounded individuals, brimming with youthful energy and a drive to innovate. It also offers an ideal path to a bright future, featuring state-of-the-art academic hubs and inspiring landscapes, with its Guangzhou International Campus reaching top levels.

Rising to challenges and striving for excellence, SCUT has charted an ambitious blueprint for reform and development in this new phase-building SCUT into a university with academic excellence, global engagement, good governance, joyful community and beautiful campuses. This marks the start of a comprehensive journey for SCUT to become a world-class university with Chinese characteristics, as it speeds its way toward the global top 100.

We warmly welcome students and scholars from around the globe to join SCUT. Let us work together to foster cultural exchange, contribute to social progress, and build a community with a shared future for all.

Organizer

华南理工大学微电子学院

Founded in 2018, the School of Microelectronics stands as one of the first schools established at the Guangzhou International Campus of South China University of Technology (SCUT) and is among the inaugural National Exemplary Schools of Microelectronics designated by the Ministry of Education. New-generation information technology serves as the engine of global development and a focal point in international scientific competition. Cultivating innovation capabilities and gathering talent advantages in integrated circuits aligns with China's major national development strategy. Responding to the nation's strategic priorities and industry demands, the School of Microelectronics was established with a profound sense of mission to nurture high-end professionals in the field of integrated circuits. In 2019, the School was recognized as one of Guangdong Province's first Exemplary Industry Schools. In 2021, the School of Integrated Circuits was formally established,and its development is being coordinated and advanced alongside that of the School of Microelectronics. In 2022, its Microelectronics Science and Engineering program was selected as a National First-Class Undergraduate Program Construction Site, marking another milestone in its academic excellence.The School currently offers two first-level doctoral degree programs (Integrated Circuit Science and Engineering, Electronic Science and Technology), two professional master's degree programs (Electronic Information and Integrated Circuit Engineering), one professional doctoral degree category (Electronic Information), and maintains two postdoctoral research stations (Electronic Science and Technology, Integrated Circuit Science and Engineering). This comprehensive academic structure establishes our institution as a leading hub for advanced education and research in electronic information technologies and integrated circuit disciplines.

Leveraging the faculty strength of the International Exemplary School of Microelectronics and recruiting outstanding talents globally, the School has established a young, internationalized, and high-caliber teaching and research team. Currently, the School has 60 faculty and staff members, including 39 full-time faculty, 3 postdoctoral researchers (with over 20 additional corporate postdoctoral researchers). Among the full-time faculty, 90% hold doctoral degrees, including 14 professors and 20 associate professors. The faculty cohort features 8 high-level overseas talents, 1 Fellow of the Royal Academy of Engineering, 4 IEEE Fellows, 1 recipient of the national major talent program, 1 recipient of the National Science Fund for Distinguished Young Scholars, 1 recipient of the National Science Fund for Excellent Young Scholars,1 Guangdong Provincial Distinguished Teacher, 1 Guangdong Provincial Outstanding Young Scholar, and 12 provincial/municipal high-level talents. Additionally, the School collaborates with industry leaders by appointing senior experts from leading enterprises as adjunct or visiting professors, creating a robust faculty team integrating academic and engineering expertise.The School's disciplines span a comprehensive spectrum covering both fundamental and applied research, forming a complete professional chain encompassing integrated circuit design-manufacturing-packaging and testing-system integration. Current research focuses on forward-looking applied fundamental studies and chip development in areas including broadband communication chips, computing and AI chips, low-power IoT chips, third-generation semiconductor devices and chips, semiconductor materials and devices, and flexible electronics. Concurrently, the School advances applied systems research in communication, radar, IoT, artificial intelligence, and medical health technologies, driving innovation across interdisciplinary domains.

The School implements a scientific talent cultivation system that emphasizes foundational disciplinary education and strengthens innovation capability development, equipping students with a robust interdisciplinary knowledge framework in microelectronics and integrated circuits. By integrating globally distinguished faculty resources and inviting internationally renowned scholars to deliver specialized courses, the institution systematically enhances students' global perspectives. As a national leader in engineering education, the School houses multiple state-level teaching and research platforms including the National Integrated Circuit Talent Training Base, National Innovation Experimental Zone for Talent Development Models, National Engineering Practice Education Center, and National Experimental Teaching Demonstration Centers. These authoritative academic infrastructures collectively provide a comprehensive ecosystem for cultivating next-generation innovators with theoretical mastery, technical proficiency, and cross-disciplinary competencies, solidifying the School's position as a national benchmark in microelectronics education.

Capitalizing on its strategic location in the Guangdong-Hong Kong-Macao Greater Bay Area—a global hub for electronic information industries—the School proactively collaborates with leading domestic enterprises and research institutes to establish joint training platforms. While conducting cutting-edge academic research, it deeply aligns with industrial demands by driving core technological innovation in integrated circuits and accelerating technology transfer, thereby achieving seamless integration of education, research, production, and application. The School implements a dual mentorship system combining academic and industrial supervisors to strengthen the cultivation of comprehensive theoretical and applied competencies, while advancing its coordinated industry-academia-research talent development initiative that bridges technological breakthroughs with real-world implementation.

The School offers a complete academic structure spanning undergraduate to doctoral programs. At the undergraduate level, it enrolls students in Microelectronics Science and Engineering and Integrated Circuit Design and Integrated Systems. Graduate programs include Microelectronics and Solid-State Electronics, along with Electronic Information. Graduates in integrated circuits are in exceptionally high demand, with the School maintaining a 100% employment rate. Over 50% of graduates pursue advanced studies through postgraduate programs or overseas research opportunities, while more than 30% secure positions at Fortune Global 500 enterprises. Notably, alumni are widely recognized by industry leaders for their technical expertise and operational capabilities, with many assuming critical roles in cutting-edge semiconductor R&D and strategic project implementation, demonstrating the program's alignment with global industry standards and workforce needs.

Organizer

华南理工大学微电子学院

应时而生已不凡，勇立潮头势更坚。成立于2018年的微电子学院，是华南理工大学广州国际校区首批建设学院，也是教育部首批国家示范性微电子学院（筹建）。新一代信息技术是世界发展的引擎，也是国际科技竞争的焦点。在集成电路领域形成创新能力和人才集聚优势，是国家的重大发展战略。聚焦国家战略布局，顺应行业技术需求，培育集成电路领域高端人才，带着强烈的使命感，微电子学院应运而生。2019年，微电子学院入选广东省首批示范性产业学院。2021年，成立集成电路学院，该院与微电子学院的建设一并统筹推进。2022年，微电子科学与工程入选国家一流专业建设点。学院现有2个一级学科博士学位授权点（集成电路科学与工程、电子科学与技术）、2个硕士专业学位授权点（电子信息、集成电路工程）、1个博士专业学位授权类别（电子信息）和2个博士后流动站（电子科学与技术、集成电路科学与工程）。

海外英才多延揽，科研骨干齐云集。依托国际示范性微电子学院的师资力量，招揽海内外优秀人才，目前学院已汇聚了一支年轻化、国际化、高水平的教学及科研团队。学院现有教职工60人，其中专任教师39人，博士后3人（另有企业博后20余人），专任教师队伍中具有博士学位的教师占90%，正高职称14人，副高职称20人。学院教师中有海外高层次引进人才8人次，英国皇家工程院院士1人，IEEE Fellow 4人，国家级重大人才工程入选者1人，国家杰出青年基金获得者1人，国家优秀青年基金获得者1人，广东省教学名师1人，广东省杰出青年基金获得者1人，省市高层次人才14人次。与此同时，学院围绕集成电路产业链条，聘请龙头企业的高端人才担任学院兼职教授或客座教授，打造学术与工程兼备的强大师资。学院学科专业分布多元，基础与应用研究齐全，形成涵盖集成电路“设计-制造-封测-整机”的专业全链条。目前正聚焦宽带通信芯片、计算和人工智能芯片、低功耗物联网芯片、第三代半导体器件与芯片、半导体材料与器件、柔性电子等领域开展前瞻性应用基础研究和芯片研制，以及在通信、雷达、物联网、人工智能、医学健康等领域的应用系统研究。

多管齐下重学研，致力创新育英才。学院实施科学的人才培养体制，注重专业基础教学，强化创新能力培养，为学生打下坚实的微电子和集成电路等交叉学科知识体系。整合海内外优秀师资，邀请海外大师授课，提升学生国际视野。学院拥有国家集成电路人才培养基地、国家级人才培养模式创新实验区、国家工程实践教育中心、国家级实验教学示范中心等教学实践基地，为创新人才培养提供坚实的平台保障。

地处粤港澳湾区，学研产用优势显。依托地处电子信息产业发达的粤港澳大湾区的优势，学院致力于与国内龙头企业和研究所共建联合培养基地，在开展前沿学术研究的同时，深度对接企业需求，在集成电路领域开展核心关键技术研究并积极推进技术转化，实现“学研产用”的深度融合。同时，实行学企双导师制，加强理论与应用的综合能力培养，深度推进“产-学-研”协同育人计划。

学生培养效果显著，优秀人才供不应求。学院本硕博专业学科齐备，本科招生专业为微电子科学与工程和集成电路设计与集成系统专业，研究生招生专业为微电子学与固体电子学专业和电子信息专业。集成电路毕业生供不应求，就业率100%，读研、出国深造比例超过50%，在世界500强企业就业人数比例超过30%，毕业生普遍受到行业龙头企业好评与重用。

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- 晶圆老化测试（WLBI）：对划片前晶圆上的芯片进行老化测试，暴露并剔除早期失效的芯片。
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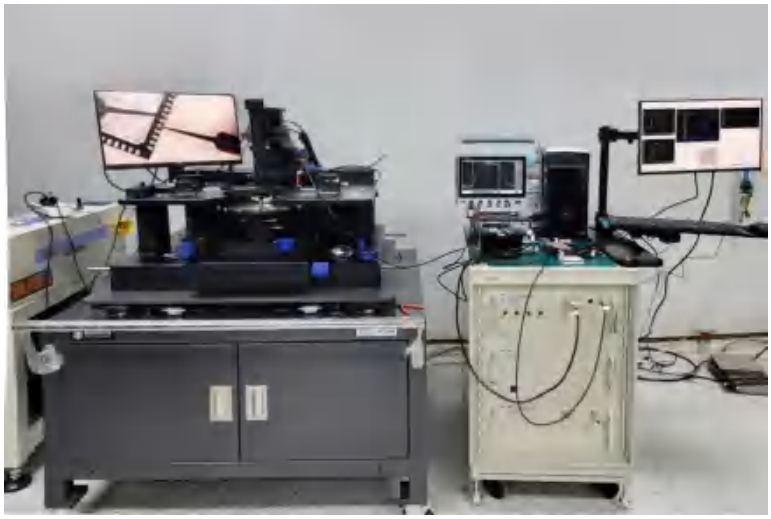

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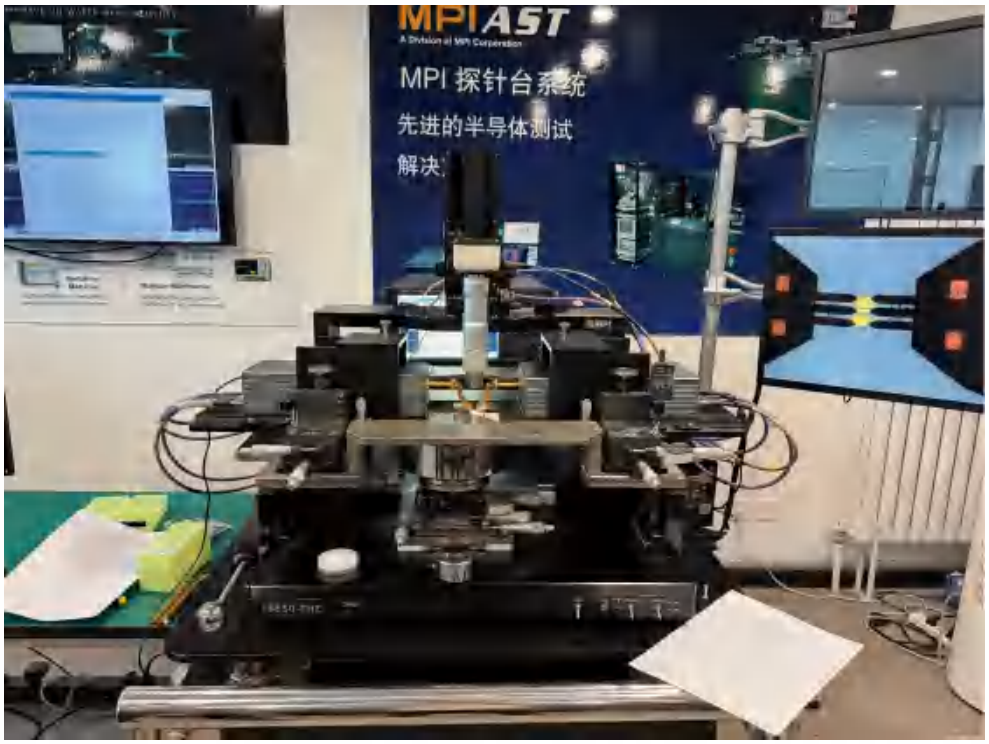

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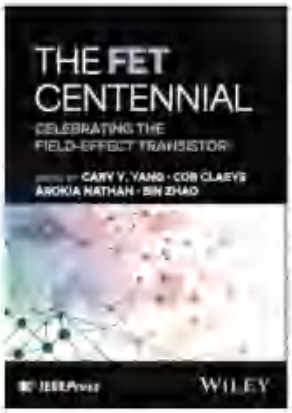

The FET Centennial: Celebrating the Field-Effect Transistor

Edited by

Cary Y. Yang, Cor Claeys, Arokia Nathan, Bin Zhao

Hardcover 978-1-394-40648-7 July 2026 **$110.00**

Presents a landmark volume documenting 100 years of field-effect transistor innovation and applications

The invention of the field-effect transistor (FET) in 1925 transformed the trajectory of modern civilization, enabling virtually every electronic device in existence today. From the earliest integrated circuits to the most advanced computers and smartphones, the FET has served as the indispensable foundation of contemporary information technology. *The FET Centennial: Celebrating the Field-Effect Transistor* commemorates this milestone by gathering a distinguished group of contributors to provide a comprehensive account of the device's history, global development, diverse applications, and potential future directions.

This unique volume begins with an in-depth exploration of the history and evolution of FET technology, including the MOSFET's rise and international advances across the United States, Europe, and Asia. The second section highlights critical applications and integration processes, ranging from memory and logic devices to CMOS image sensors, analog/RF CMOS, and emerging thin-film and wide-bandgap transistors. The final section addresses state-of-the-art developments, such as 3D and gate-all-around FETs, nanoscale transport phenomena, and the incorporation of novel 2D materials, while considering the possibility of what is next for FET and what might come after.

A singular resource that not only documents a century of achievements but also contextualizes the field-effect transistor's enduring importance and likely trajectory in the decades ahead, *The FET Centennial*

- Addresses both historical milestones and technological disruptions shaping current and future electronics
- Examines international research and development with narratives from the United States, Europe, and Asia
- Covers device structures from MOSFETs to III-V and 2D-material-based FETs
- Includes forward-looking analyses of nanoscale transport, 3D architectures, and GAAFET innovations
- Features detailed coverage of process integration, interconnects, lithography, and compact modeling

Authored by globally recognized experts with leadership roles in academia, industry, and professional societies, *The FET Centennial: Celebrating the Field-Effect Transistor* is essential reading for graduate and senior undergraduate students in electrical engineering, materials science, and applied physics courses such as Semiconductor Devices, Integrated Circuit Technology, and Microelectronics. It is also an indispensable reference for researchers, practicing engineers, and historians of science and technology.

Cary Y. Yang, PhD, is Professor of Electrical and Computer Engineering at Santa Clara University. An IEEE Life Fellow, he has served as Editor of *IEEE Transactions on Electron Devices*, President of the IEEE Electron Devices Society, and as a member of the IEEE Board of Directors. His research spans silicon-based nanoelectronics, nanocarbon interconnects, and nanostructure interfaces.
Cor Claeys, PhD, is Professor at KU Leuven, Belgium, and teaches internationally in Europe, China, India, and Brazil. A Fellow of both the Electrochemical Society and IEEE, he has co-edited books on low-temperature electronics and germanium-based technologies, authored four monographs, and contributed more than 1,400 technical papers and 16 book chapters.
Arokia Nathan, PhD, is Bye-Fellow and Tutor at Darwin College, University of Cambridge. With over 600 publications, six books, more than 150 patents, and four spin-off companies, he is a Fellow of the IEEE, IET (UK), Royal Academy of Engineering, Canadian Academy of Engineering, Society for Information Displays, and a Foreign Member of the Chinese Academy of Sciences. His research has advanced TFT and sensor technologies.
Bin Zhao, PhD, has been with SEMATECH, Rockwell, Conexant, Skyworks, Freescale, Fairchild, and OnSemi in advanced IC technology and product development. An IEEE Fellow, he holds over 100 patents and has served as Founding Co-Chair of the RF/AMS Working Group for the International Technology Roadmap for Semiconductors, IEEE Conferences Committee Chair, and President of the IEEE Electron Devices Society.

100 YEARS FIELD-EFFECT TRANSISTOR

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"The FET Centennial – Celebrating the Field-Effect Transistor"

Cary Y. Yang, Cor Claeys, Arokia Nathan, and Bin Zhao, editors

A Special Tribute in Memory of Chih-Tang Sah [1932-2025] (Jack Sun)
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Note

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